V202 DELAY MODULE

FUNCTIONAL DESCRIPTION

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INTRODUCTION

The V202 Delay Module is a replacement for the V102 Delay Module. The V102 can no longer be manufactured due to parts obsolescence.

The V202 has several upgrades in comparison to the V102. The most significant of these changes is PPM capability. The V202 may be programmed for up to eight users. Other upgrades include the use of 32-bit counters instead of 16-bit counters for the pulse widths, the ability to clock the pulse delays and pulse widths with timeline events (Event Link words) rather than a conventional clock, and an increase in the number of programmable interrupts.

The V202 is the same form and fit as the V102, a standard 6U VME module. However, existing software used to support the V102 cannot be used with the V202. New software has been written to support operation of the V202.

ASSOCIATED DRAWINGS

94028890	V202 Schematic
94028891	V202 Drill Detail
94028892	V202 PCB Assembly
94028893	V202 Front Panel Detail
94028894	V202 Module Assembly
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OVERVIEW

The primary function of the V202 module is to decode the Event Link, and trigger any of up to eight TTL compatible pulse outputs upon the reception of specific Event Link words. Triggering can also be accomplished through the use of an external signal, a VME command, or the start or end of the pulse output of a previous channel. A gated mode is also available, where the pulse output of a channel is triggered by the start of the previous channel's output, and ended by its own programmed output point.

The pulse outputs themselves are defined by two parameters: delay and width. The delay is the time between the trigger event and the start of an active pulse output. The width is the actual duration of an active pulse. The delay time and width time for each channel are controlled through the use of individual 32-bit down counters.

Each of the eight output channels has its own set of controlling bits and registers. Each channel can use a different trigger mode, and be triggered by different events. Each channel's output can be turned on or off, or set active high or active low. Each channel's delay and width counters can be programmed to use different clocks: 10MHz, 1MHz, an external clock (up to 5MHz), or an event clock. When a clock is chosen for a channel, that clock is used for both the delay counter and width counter of that channel. The only time that the delay and width counters of the same channel may use different clocks is when the board is jumped to AGS mode.

The V202 module is configured by programming its various registers and memory locations through the VME interface. At power up, the EPLD registers and memory contain zeros. Once configured, the V202 is self-supporting. It will continue to function until power is removed. It will not maintain its configuration through a power cycle.

For the purposes of this document:

- A pulse output is defined as the output at the connector itself. An output channel is defined as all the registers, controls, and connectors that are used to create a pulse output.

- An active pulse is defined as a pulse output whose state has actually changed, or when an output channel's width counter has been started. A pulse output is not considered active while its delay counter is running.

- An active channel is defined as a channel that has been triggered, and whose active pulse has not yet been terminated.

- An operator is defined as the person or persons responsible for configuring and using the V202 module.

- A user is defined as any one of eight sets of configurations that can control the V202 module. Users switch upon the occurrence of specific Event Link words.

FRONT PANEL LED INDICATORS

There are several front panel LEDs that provide visual status indications of basic module functions.

Power

The topmost green POWER indicator gives visual verification that the onboard power is present. It is tied to the +5V power acquired from the VME backplane.

VME

The green VME indicator lights up whenever a VME data transfer occurs between the V202 module and the VME controller. It is essentially tied to *DTACK, but it is pulse stretched in order to be easily observable.

No Lock

The red NO LOCK indicator turns on when the V202 module's PLL is not synchronized to the Event Link. Under normal working conditions, this indicator will not be illuminated.

Event Link

The green EVENT LINK indicator lights up whenever a valid Event Link word is decoded. The input to this LED is also pulse stretched, which makes it easier to be observed. Under normal working conditions with an active Event Link, this LED will be illuminated. It will never be on when the red NO LOCK indicator is on.

Pulse Outputs

Each of the 8 pulse outputs has a small green activity indicator. Whenever a pulse output activates, its corresponding LED will be illuminated. The inputs to these LEDs are pulse stretched, so that even very short pulse outputs will be easily observable.

If a channel uses a very small delay, and it is re-triggered immediately after finishing an output pulse, the corresponding LED will not have time to turn off and on again. This gives the appearance of one long continuous pulse, although the pulse output does indeed turn off prior to returning to the active state.

FRONT PANEL CONNECTORS

4 External Trigger Inputs

The four topmost LEMO type connectors on the front panel are used for external trigger inputs. If no external trigger inputs are used, these connectors can remain unconnected.

Each of the external trigger inputs is used for 2 channels. TRG 1/2 is used to trigger channels 1 and 2. TRG 3/4 is used for channels 3 and 4. TRG 5/6 is used for channels 5 and 6. TRG 7/8 is used for channels 7 and 8.

A positive going edge on an external trigger input will initiate the trigger sequence.

The trigger inputs are optically isolated from the rest of the module.

External Clock Input

The external clock input LEMO connector (CLK) is found directly below the four external trigger connectors.

When any of the eight output channels are programmed to use an external clock, this is the optically isolated source from where it is derived.

The maximum rate of the external clock is 5MHz.

Event Link Input

The Event Link is brought into the V202 module through this BNC twinax connector. The PLL onboard the V202 will correctly accept the Event Link even if the connector is wired with incorrect polarity.

The Event Link input is transformer coupled.

8 Pulse Outputs

The bottom eight LEMO connectors are for the individual pulse outputs. Channel 1 is the topmost of these eight connectors. Channel 8 is the bottom connector.

Each of the eight outputs is driven by a 50Ù line driver. The outputs all have short circuit protection. They may be wire-ORed, but the outputs must not be programmed for inverted operation if doing this. All outputs are TTL compatible.

BACKPLANE CONNECTORS

There are two 96-pin backplane connectors on the V202 module used to interface with the VME bus. They are designated P1 and P2. In addition to the standard VME power, ground, address bus, data bus, and control bus lines, there is some used defined I/O.

An alternate Event Link input is available on pins 12 and 13 of backplane connector P2A. To use this Event Link input, pins 2 and 3 of the jumper header JP2 must be shorted together. Pin 1 of this jumper header must be left open. To use the front panel connector for the Event Link input, pins 1 and 2 of jumper header JP2 must be shorted together, and pin 3 must be left open.

Provisions have also been made to have the eight pulse outputs available on the backplane. Pulse outputs 1 through 8 are wired consecutively from P2A-24 to P2A-31. These provisions are made primarily for the TTL TO AGS Converter interface, but they made be used for other purposes.

In addition to the eight pulse outputs, there are several specially formatted clocks available on P2. They are 1MHz, 100KHz, 10KHz, and 1KHz. These clocks are derived from the Event Link. If the Event Link is not connected, the onboard PLL will continually search for lock, and the clock frequencies will appear to wander. These clocks are available primarily for the TTL TO AGS Converter interface, but they may be used for other purposes.

The four clocks do not have a 50/50 duty cycle. Rather, they are short, active low strobes occurring at their respective frequencies. Their characteristics are described below.

1 MHz
P2A-20 is the 1MHz output. P2A-16 is the inverted representation of 1MHz. The 1MHz output is active low. The negative going pulse is 100 nanoseconds in length, occurring once every microsecond.

100 KHz
P2A-21 is the 100KHz output. P2A-17 is the inversion of 100KHz. The 100KHz output is active low. The negative going pulse is 1 microsecond in length, occurring once every 10 microseconds.

10 KHz
P2A-22 is the 10KHz output. P2A-18 is the inversion of 10KHz. The 10KHz output is active low. The negative going pulse is 1 microsecond in length, occurring once every 100 microseconds.

1 KHz
P2A-23 is the 1KHz output. P2A-18 is the inversion of 1KHz. The 1KHz output is active low. The negative going pulse is 1 microsecond in length, occurring once every millisecond.

VME INTERFACE

The V202 module uses bits A23-A1 for addressing. To avoid potential conflicts with other types of boards that may reside in the same VME chassis, the following base addresses are reserved for V202s: 030000h, 040000h, 050000h, 060000h, 070000h, 080000h, 090000h, and 0A0000h. Base address 03 should be assigned to the first V202 module in a chassis, followed by 04, 05, and so on. The V202 module uses SW1, an 8-position SIP switch, to set the board's base address. SW1 is clearly marked to facilitate setting the proper address.

During a VME data transfer, when address bits A23-A16 match the settings of SW1, the V202 module will respond. Bits A15-A1 are decoded within the EPLD to access the various registers and memory locations on the board. The DS0* and DS1* VME signals essentially represent a virtual A0 address line. When DS0* is low, data lines D7-D0 are active. When DS1* is low, data lines D15-D8 are active. When DS0* and DS1* are low simultaneously, all sixteen data lines are active.

There are two valid address modifier codes that will be recognized by the V202 module: 39h and 3Dh.

Some of the registers in the V202 module can be accessed using D16 and D08(EO) data transfers. However, there are certain registers and memory locations that only contain eight bits of useful content. These areas always use the low data byte, at odd addresses. See appendix A for a list of valid addresses and their assignments.

The bit positions of a 16-bit register are referenced as follows:

MSB—D15.D14.D13.D12.D11.D10.D9.D8 D7.D6.D5.D4.D3.D2.D1.D0—LSB
High Byte Low Byte

Only the standard Read/Write cycle data transfer is supported by the V202. All transfers are terminated through the use of DTACK*.

Most registers, and all memory locations, are read-write capable. There are several read-only and write-only registers. Attempting to write to a read-only register will not cause a VME problem…the register just won't accept the data. Attempting to read a write-only register will most likely retrieve a value of FFh, but that is not guaranteed. This is because the data lines of the VME bus will be in a tri-stated condition at the time of the read.

Any attempt to read or write a non-existing address location on the V202 will be similar to writing to a read-only register, or reading from a write-only register. The board will respond with DTACK*, but no actual data will be exchanged.

The V202 is a VME bus slave, and cannot initiate VME bus transfers. It cannot respond to read-modify-write cycles, or block transfer cycles.

BOARD IDENTIFICATION

The V202 module may be identified remotely by reading the VME ID message programmed into the V202 module's EPLD. The message identifies the module type, serial number, and revision letter of the module. It resides in a read-only register area of the EPLD, from address 0000h to 001Fh. The contents of these registers are ASCII representations.

Starting at address 0000h, the VME ID should read as follows:

VMEIDBNLV202(sp)(sp)REVx(sp)(sp)SER#xxxx(sp)(sp)(sp)(sp)

(sp) is an ASCII space character.

The serial number and revision letter are derived from onboard shorting sockets SS1 and SS2 respectively. The shorting sockets have the appropriate jumpers soldered into them when the board is populated. The jumpers essentially constitute binary counts for both the serial number and the revision letter.

If there are no jumpers in SS1, the serial number of the board is 1. If one jumper is soldered into the LSB position of SS1, the serial number of the board is 2, and so on. There are eight jumper positions in SS1, allowing for serial numbers 1 through 256.

If there are no jumpers in SS2, the revision letter of the board is A. If one jumper is soldered into the LSB position of SS2, the serial number of the board is B, and so on. There are three jumper positions in SS2, allowing for revision letters A through H.

Both SS1 and SS2 have the letters "LSB" embossed on the board adjacent to their least significant bit positions.

PPM FUNCTION

Unlike the V102, the V202 module has PPM, or multiple user capability. The V202 may be configured with up to eight individual users. For the purposes of this document, the eight users are identified as User 1 through User 8.

When the V202 module is first powered up, it defaults to User 1. A system reset will also re-initialize the board to User 1. If PPM capability is not enabled, the V202 board will operate using only the User 1 registers and settings. If PPM capability is disabled after being enabled, the V202 board will revert back to the User 1 settings, regardless of what user it was operating in when the PPM capability was disabled.

Most programmable settings of the V202 module can be configured on a user basis. In other words, each user has a unique set of control registers for V202 configuration. A user's register set is enabled when that user is active. The user programmable settings include channel clock, clock events, trigger mode, output mode, gate mode, pulse delay, and pulse width. In addition, each user has a separate trigger event lookup table.

There are several control registers that are global in nature. These registers are active across all users. They include the Interrupt Level register, the Interrupt Vector register, the Interrupt Enable register, the Clock Resync Code register, the Pulse Arm register, the Pulse Trigger register, and the Reset register.

To configure the V202 module for multiple users the following steps must be taken:

1) Enable PPM function
2) Define User Switch Code
3) Enable specific users (It is recommended that User 1 always be enabled, since this is the default user)
4) Define User Codes

PPM capability is enabled by setting D8 of the 16-bit User Switch register to a value of 1. If D8 of this register is zero, PPM capability is disabled. The User Switch register is located at address 0040h and 0041h.

The User Switch Code is entered into D7->D0 of the User Switch register. This defines the Event Link word upon whose occurrence the user will switch.

To enable specific users, D8 of the corresponding 16-bit User Code registers must be set to a value of 1. If D8 of a particular register is zero, that user is disabled. The User 1 Code register occupies address 0042h and 0043h. The User 2 Code register occupies address 0044h and 0045h, and so on, up to the User 8 Code register, which occupies address 0050h and 0051h.

The individual User Codes are entered into D7->D0 of the corresponding User Code register. This defines the Event Link word that determines the next user the V202 module will switch to.

When an Event Link word matches one of the enabled User Codes, the V202 prepares to switch to that user. The actual point that the switch takes place is when the User Switch Code appears on the Event Link. During the switch all eight channels are reset. Any active pulse outputs are terminated. The new user's delay and width times are loaded into each channel's counters, the new user's trigger event lookup table is activated, and the new user's control register set becomes active. As described earlier, this affects the channel clocks, clock events, trigger modes, output modes, gate modes, pulse delays, and pulse widths. All these new settings remain in affect until the user is switched again.

If multiple User Codes appear on the Event Link prior to the occurrence of the User Switch code, the last User Code seen defines which user will become active. If the latest User Code to appear is the same as the board's current user, no action will be taken upon the receipt of the User Switch code. If no User Code appears prior to the receipt of the User Switch code, no action will be taken.

Care should be taken when an Event Link word defined as the User Switch Code is also defined as a user's Clock Event Code. Assuming the User Switch Code always, or almost always, causes a user switch, the resetting of all channels makes the User Switch Code virtually useless as a Clock Event Code. However, if the occurrence of the User Switch Code does not often produce a user switch, it might make sense to use the User Switch Code as a user's Clock Event Code.

During a user change, if the user being vacated is using a matching Clock Event Code, that user will see a clock pulse just prior to the change. However, fifty nanoseconds later all the channels are reset. If the user being activated is using a matching Clock Event Code, that user will not see a clock pulse during the user change. Once a user is active, the occurrence of a matching User Switch Code will generate a clock pulse for that user.

The same concerns exist if the User Switch Code is programmed into the Event Link look-up table for channel triggering. Since all the channels are reset during a user change, no triggering of channels can take place during that period. However, if the occurrence of the User Switch Code does not produce a user switch, no reset occurs, in which case the User Switch Code can trigger a channel.

The Status register located at address 0026h and 0027h includes three bits that identify the current user. However, it is possible that the users are being switched rapidly; so trying to find out if a particular user has been activated may be difficult. To make this easier to do, the V202 module has an 8-bit User History register, located at address 0053h. Each bit of this register represents a user. D0 represents User 1, D1 represents User 2, and so on. Whenever a user is activated, its bit in the User History register is set to a value of 1. If a user is never activated its bit remains at zero.

The History register is not cleared with a system reset. Nor is it cleared automatically when the register is read. Instead, writing a value of 1 to a bit position within the register will clear that bit. Multiple bits can be cleared simultaneously. Writing a value of 0 to a bit position will have no affect.

EVENT LINK DECODING

The bi-phase mark encoded Event Link can be brought into the V202 module through the front panel connector, or through the backplane on pins P2A-12 and P2A-13. The 2-position jumper header, JP2, determines the source. If pins 1 and 2 are shorted, the input will be from the front panel. If pins 2 and 3 are shorted, the input will be from the backplane. If no pins are shorted, the V202 module will not see the Event Link.

The V202's onboard PLL synchronizes to the Event Link and provides NRZ-L data and a 10MHz clock. The positive going edge of the 10MHz clock is in the middle of each NRZ-L bit cell. As long as the PLL is synchronized to the Event Link, the red front panel NO LOCK indicator will be off. If the PLL loses synchronization, NO LOCK indicator will be on. There will be "noise" on the data line, and the clock will drift.

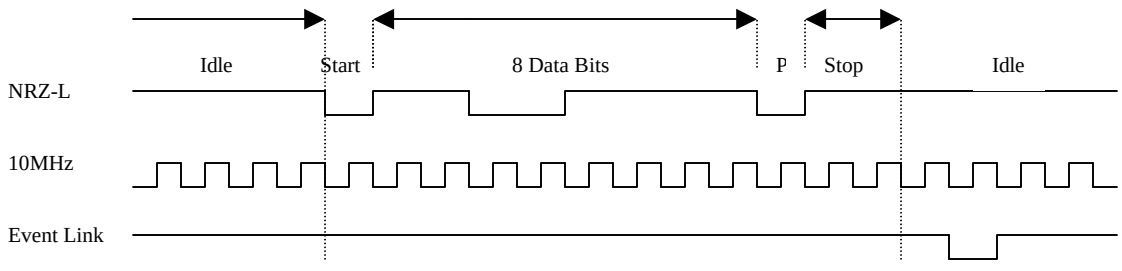
Once synchronized, the V202 will continually try to decode valid Event Link words. If the Event Link is running but there are no data words, it is in the idle state. The NRZ-L data will produce a string of "1"s. However, the 10MHz clock will still be locked. In this condition, the NO LOCK indicator will be off, but so will the green EVENT LINK indicator. As actual Event Link words appear, the bi-phase mark encoded data gets decoded into NRZ-L data. Each data word is tested to determine if it is valid. The determination of a valid word is based on the following conditions:

1) Word preceded by 2 high bits (idle bits, or the previous word's stop bits)
2) Start bit (low)
3) 8 data bits
4) Parity bit (even)
5) 2 stop bits (high)

After decoding, the Event Link word is checked for matches in applicable registers. It is also used for the Event Link look-up table, to determine if an output should be triggered. If all but the parity condition is met, a parity error occurs. If enabled, a parity interrupt will be generated. The word is not passed to the registers or the look-up table. If any other conditions are not met, the Event Link word is considered invalid, and is ignored.

A valid Event Link word produces a negative going Event Link strobe. This strobe is pulse stretched and used to light the EVENT LINK indicator. A steady stream of valid Event Link words will cause the EVENT LINK indicator to be on continuously.

The figure below shows the internal timing relationship of the Event Link decoding process, after the PLL has converted the bi-phase mark Event Link data to NRZ-L.



ARMING PULSE OUTPUTS

The 8-bit Pulse Arm register is located at address 002Bh. This is a global register, applied across all users. Each bit of the Pulse Arm register corresponds to one of the pulse outputs. D0 arms pulse output 1, D1 arms pulse output 2, and so on. If a Pulse Arm bit is zero, it is not armed and its corresponding output can never be triggered. The unarmed, or off state of the output, high or low, is determined by the contents of the current user's Output Mode register.

When a Pulse Arm bit is set to a value of 1, the current user's delay and width values are immediately loaded into that channel's counters, and the channel is ready to be triggered.

The Pulse Arm register should be the last register written to when configuring the V202 module. This will prevent inadvertent triggers due to incomplete register settings.

DELAY AND WIDTH COUNTERS

The delay and width of each pulse output is determined by that channel's own delay and width counters. Both the delay and width counters are configured as 32-bit count down counters. When a channel is triggered, its delay counter begins to count down from a pre-loaded value. As soon as the delay counter reaches zero, the pulse output is activated and the channel's width counter starts to count down from its pre-loaded value. When the width counter reaches zero the pulse output is terminated.

Delay and width values are loaded into a channel's counters upon the following conditions:

1) When the channel is armed
2) When the channel is reset
3) When a system reset is issued
4) When a user changes
5) When a channel's active pulse ends

Storage must be provided for the delay and width values of each channel. Since there are eight users, with eight channels per user, each requiring 32-bits of delay values and 32-bits of width values, a total of 512 bytes of memory are required. Each channel's block of memory must be accessible independently of the other channels, because the V202 module must be able to perform simultaneous loads of channels. In addition, the VME controller must be able to write new values into this memory without interrupting the normal loading operation of the delay and width values. This means that the storage for the delay and width values must be comprised of blocks of dual-port RAM. These constraints, along with the physical constraint of the EPLD, are the reasons that the delay and width values are stored in byte increments. See appendix A for a VME memory map of the storage area.

Loading the delay and width values of each channel is performed in a specific eight-step sequence. Each step of the sequence loads one byte at a time. The entire sequence takes about 900 nanoseconds.

1) Load the most significant byte of the delay value (Delay bits 31->24)
2) Load next most significant byte of the delay value (Delay bits 23->16)
3) Load next most significant byte of the delay value (Delay bits 15->8)
4) Load the least significant byte of the delay value (Delay bits 7->0)
5) Load the most significant byte of the width value (Width bits 31->24)
6) Load next most significant byte of the width value (Width bits 23->16)
7) Load next most significant byte of the width value (Width bits 15->8)
8) Load the least significant byte of the width value (Width bits 7->0)

The delay and width values for each channel are stored sequentially in memory in order to expedite the loading process.

The delay and width counters can be clocked with a 10MHz clock, a 1MHz clock, an external clock (up to 5 MHz), or an event clock.

The lowest acceptable value for a channel pulse output delay is zero. This means that the output will become active immediately upon being triggered. The highest acceptable value for a channel's delay count is FFFFFFFFh, or 4,294,967,295. Using this count and the 10MHz clock will provide a delay of about 429.5 seconds, or 7.16 minutes. Using this count and the 1MHz clock will provide a delay of about 71.6 minutes.

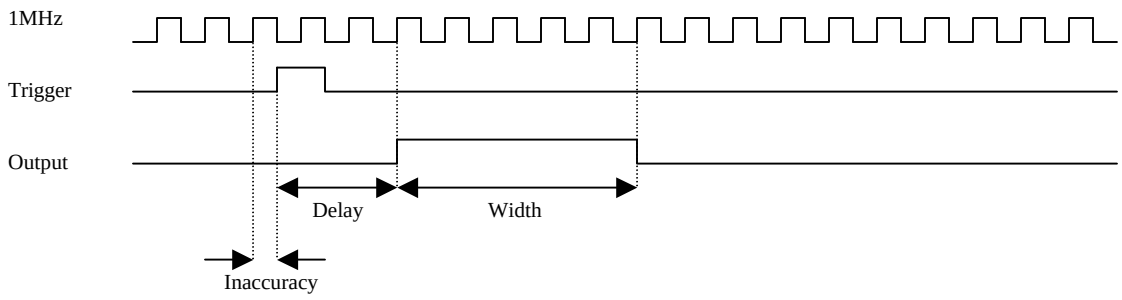
The lowest acceptable value for a channel pulse output width is 1. A pulse cannot have a width of zero. This also means that a width value of zero will provide the longest pulse, because the counter will roll over from zero to FFFFFFFFh and count down from there.

When using a pulse delay of any non-zero value, the delay can have a built in inaccuracy of up to –1 clock period. When a channel is triggered, the delay counter is enabled. The first occurring positive clock edge after that will start to decrement the counter. Since in certain cases there is little or no synchronization between the trigger point and the counter's first clock edge, the delay has an uncertainty of up to -1 clock. This is less true when using the Event Link for the trigger and the 10MHz clock for the delay counter. Since the 10MHz clock is derived from the Event Link, the time between the trigger and the first clock edge will be constant. It won't quite be a full clock period, due to internal delay paths, but it will be a fixed amount of time. In this case the delay will be constant and repeatable in reference to the trigger.

Because the width counter uses the same clock as the delay counter, and the delay counter is essentially cascaded into the width counter, any non-zero pulse delay value will result in a constant and repeatable pulse width. However, if the pulse delay is set to zero, the prior explanation for the pulse delay variance will now be applicable to the pulse width. There can be an inaccuracy of up to –1 clock period, depending on the combination of trigger source and clock source. This could be a problem if the programmed pulse width is one. However, internal circuitry guarantees that the narrowest pulse width is at least ½ clock period in duration.

Any active pulse output will be terminated by a reset, and the delay and width counters will be reloaded with the current user's values for that channel.

The figure below shows an example timing relationship between a trigger and pulse output. The delay value is three and the width value is five.



CLOCKING WITH AN EVENT

The V202 module can generate a 200 nanosecond pulse on each occurrence of a specific Event Link word. This pulse, called the event clock, may be used to clock the delay and width counters of each channel. One unique event clock may be programmed for each user. That event clock may then be applied to any or all of the channels.

Each user's Clock Event Code is entered into D7->D0 of the corresponding 8-bit User Clock Event register. This code defines the Event Link word that will produce an event clock. The User 1 Clock Event register occupies address 0071h. The User 2 Clock Event register occupies address 0073h, and so on, up to the User 8 Clock Event register, which occupies address 007Fh.

Normally, an Event Link word defined as the User Switch Code should not be used for any of the Clock Event Codes. Since all channels are reset during a user switch, the User Switch Code can be essentially useless as a Clock Event Code. However, if the occurrence of the User Switch Code does not often produce a user switch, it might make sense to use the User Switch Code as a user's Clock Event Code.

If the user being vacated is using a matching Clock Event Code, that user will see a clock pulse fifty nanoseconds prior to the user change. If the user being activated is using a matching Clock Event Code, that user will not see a clock pulse during the user change. Once a user is active, the occurrence of a matching User Switch Code will generate a clock pulse for that user.

SELECTING CLOCKS

Clocks are used for the delay and width counters of each channel. The frequency of the selected clock, along with the delay and width values loaded into a channel's counters, determines the actual delay time and duration of a pulse output.

There are four clocks to select from when configuring a channel. They are 10MHz, 1MHz, external clock, or event clock. There is only one external clock, brought into the V202 module through a front panel connector, and is limited to 5MHz. Each channel within a user can be programmed to use any of the four clocks. A different user may select a different set of clocks for the eight channels. Although the external clock doesn't change from user to user, the event clock can be different.

The User 1 output channels have their clocks selected by the 16-bit User 1 Clock Mode register, which is located at address 0060h and 0061h. The User 2 output channels have their clocks selected by the 16-bit User 2 Clock Mode register, which is located at address 0062h and 0063h, and so on, up to the User 8 Clock Mode register, which is found at address 006Eh and 006Fh.

Each channel has its clock mode determined by two bits within the active user's Clock Mode register. Bits D1 and D0 control channel 1. Bits D3 and D2 control channel 2, and so on. The two bits are decoded as follows:

D3	D2	Channel 2
0	0	10MHz
0	1	1Mhz
1	0	External Clock
1	1	Event Clock

D1	D0	Channel 1
0	0	10MHz
0	1	1Mhz
1	0	External Clock
1	1	Event Clock

D7	D6	Channel 4
0	0	10MHz
0	1	1Mhz
1	0	External Clock
1	1	Event Clock

D5	D4	Channel 3
0	0	10MHz
0	1	1Mhz
1	0	External Clock
1	1	Event Clock

D11	D10	Channel 6
0	0	10MHz
0	1	1Mhz
1	0	External Clock
1	1	Event Clock

D9	D8	Channel 5
0	0	10MHz
0	1	1Mhz
1	0	External Clock
1	1	Event Clock

D15	D14	Channel 8
0	0	10MHz
0	1	1Mhz
1	0	External Clock
1	1	Event Clock

D13	D12	Channel 7
0	0	10MHz
0	1	1Mhz
1	0	External Clock
1	1	Event Clock

Under normal circumstances, when a clock is selected it is applied to both the delay and width counters of a channel. The only exception is when jumper header JP10 is left open, putting the V202 module in AGS mode.

AGS mode requires that the pulse outputs be short, negative going strobes. The delay widths can still be programmed as desired. To make sure the outputs are always short strobes, two things are done internally to the configuration.

First, only the 10MHz and 1MHz clock selections are valid. If the external clock or event clock is selected, the width counters are forced to use the 10MHz clock instead. This is done regardless of the settings in the active user's Clock Mode register.

The delay counters will still use the selected clock.

Second, the value loaded into all the active width counters is forced to one, regardless of the value stored in the channels' width storage area. This guarantees that an active pulse will only be one clock period long.

The delay counters can still be loaded with any programmable value.

These constraints assure that the pulse outputs will be either 100 nanoseconds long if using the 10MHz clock, or 1 microsecond long if using the 1MHz clock.

TRIGGERING WITH AN EVENT

The V202 module can generate a trigger for any or all of the eight channels upon the occurrence of any Event Link word. This is accomplished through the use of an Event Link look-up table. Each user.

An Event Link word defined as the User Switch Code should not be programmed into the Event Link look-up table in order to trigger a channel. When the V202 module switches users, all the channels are reset. No triggering can take place during that reset period. However, if the occurrence of the User Switch Code does not produce a user switch, the User Switch Code can trigger a channel.

The Event Link look-up table resides in a separate 2K x 8 dual-port RAM device. Each user has its own block within the Event Link look-up table that requires 256 bytes of memory. The RAM device has two sets of addresses and two sets of data lines. One set is used for VME read and write communication, and one set is used to provide trigger information to the onboard EPLD. The EPLD side of the dual-port RAM is hard wired for read operation only, and is enabled at all times.

The lower eight bits of addressing for the EPLD side of the RAM is made up of the decoded Event Link words, and the upper three bits of addressing consists of the 3-bit user code. User 1 is represented by a 3-bit code of 000, User 2 is represented by a 3-bit code of 001, and so on. This part of the address does not change unless the user changes. The Event Link part of the address changes with the occurrence of each new Event Link word.

Since an Event Link word is eight bits long, there can be a maximum of 256 unique Event Link words. Using 256 bytes of memory, each Event Link word can be mapped to a data byte within the RAM. Upon the occurrence of each new Event Link word, the mapped data byte is presented to the EPLD as trigger control for each of the eight channels.

Each bit within a mapped data byte corresponds to an output channel. D0 corresponds to channel 1, D1 corresponds to channel 2, and so on. When a mapped data byte is sent to the EPLD and a bit is set to a value of 1, the corresponding channel is triggered. If a bit is set to a value of zero, the corresponding channel is not triggered.

As a minimum the entire Event Link look-up table should be initialized to all zeros prior to arming any channels. This will prevent false triggers from occurring once the V202 module starts to decode the Event Link. Ideally, initializing the Event Link look-up table would be a two-step process. First, clear the entire look-up table. Second, program those data bytes necessary to provide the intended triggers. Due to the utilization of a dual-port RAM, the look-up table may be modified during normal operation of the V202 without adversely affecting its trigger performance.

See appendix A for a VME memory map of the Event Link look-up table.

SELECTING TRIGGERS

There are four trigger methods to select from when configuring a channel. They are the Event Link, the external trigger, the previous channel's output start, or the previous channel's output end. Each channel within a user can be programmed to use any of the four triggers. A different user may select a different set of triggers for the eight channels.

There are four external trigger inputs, TRG 1/2, TRG 3/4, TRG 5/6, and TRG7/8. They are brought into the V202 module through front panel connectors. If channel 1 or channel 2 is programmed to use an external trigger, it comes from the TRG1/2 input. If channel 3 or channel 4 is programmed to use an external trigger, it comes from the TRG3/4 input, and so on.

The User 1 output channels have their triggers selected by the 16-bit User 1 Trigger Mode register, which is located at address 0080h and 0081h. The User 2 output channels have their triggers selected by the 16-bit User 2 Trigger Mode register, which is located at address 0082h and 0083h, and so on, up to the User 8 Trigger Mode register, which is found at address 008Eh and 008Fh.

Each channel has its trigger mode determined by two bits within the active user's Trigger Mode register. Bits D1 and D0 control channel 1. Bits D3 and D2 control channel 2, and so on. The two bits are decoded as follows:

D3	D2	Channel 2	D1	D0	Channel 1
0	0	Event Link	0	0	Event Link
0	1	External	0	1	External
1	0	Previous Channel Start	1	0	Previous Channel Start
1	1	Previous Channel End	1	1	Previous Channel End

D7	D6	Channel 4	D5	D4	Channel 3
0	0	Event Link	0	0	Event Link
0	1	External	0	1	External
1	0	Previous Channel Start	1	0	Previous Channel Start
1	1	Previous Channel End	1	1	Previous Channel End

D11	D10	Channel 6	D9	D8	Channel 5
0	0	Event Link	0	0	Event Link
0	1	External	0	1	External
1	0	Previous Channel Start	1	0	Previous Channel Start
1	1	Previous Channel End	1	1	Previous Channel End

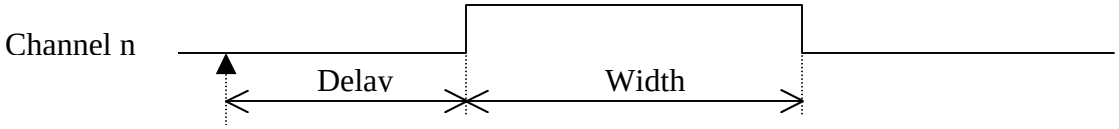
D15	D14	Channel 8	D13	D12	Channel 7
0	0	Event Link	0	0	Event Link
0	1	External	0	1	External
1	0	Previous Channel Start	1	0	Previous Channel Start
1	1	Previous Channel End	1	1	Previous Channel End

When channel 8 is programmed to trigger with a previous channel start or a previous channel end, it triggers on the start or end of channel 7's output. When channel 7 is programmed to trigger with a previous channel start or a previous channel end, it triggers on the start or end of channel 6's output. However, there are no channels previous to channel 1. Attempts to program a previous channel trigger for channel 1 will be forced to an external trigger, regardless of the settings of D0 and D1 in the active user's Trigger Mode register.

Once triggered, a channel cannot be triggered again until the active pulse ends, unless it is terminated by a reset. Attempts to trigger an active channel will not extend the pulse delay or the pulse width of the output pulse.

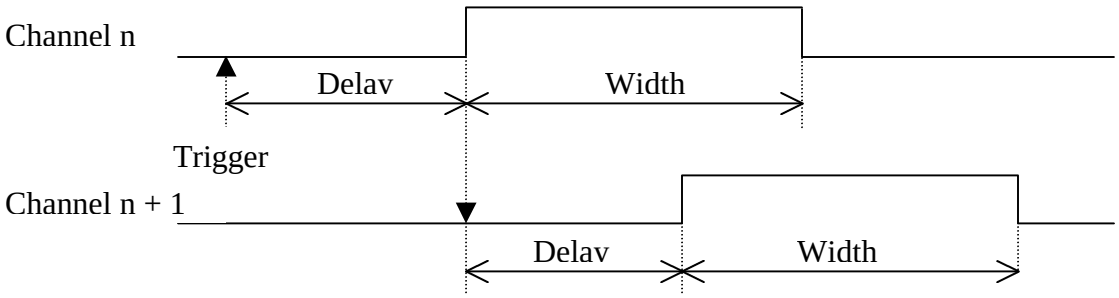
The figures below show examples of the different triggering methods.

1) Event Link or External Trigger

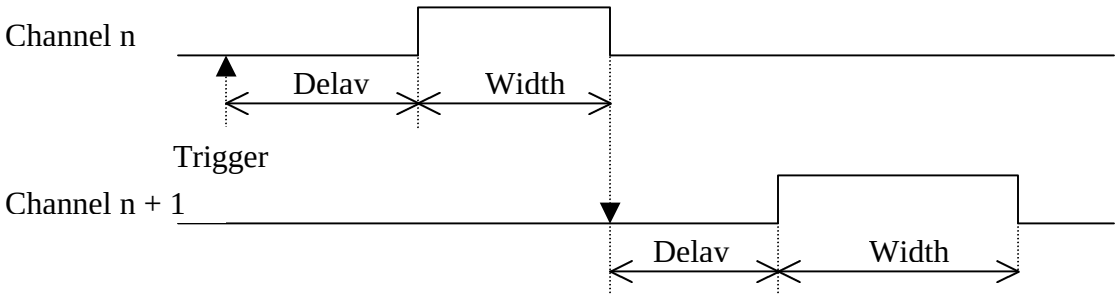


Trigger from:
* Event Link
* External input

2) Previous Channel Start Trigger



3) Previous Channel End Trigger



SELECTING OUTPUT MODE

The output mode of a channel determines whether a pulse output is active high (normal) or active low (inverted). The output mode can also be used to turn a channel's output off, preventing any pulses from occurring.

Each channel's output within a user can be independently controlled. A different user may select different output modes for any of the eight channels.

The User 1 output channels have their output modes selected by the 16-bit User 1 Output Mode register, which is located at address 00A0h and 00A1h. The User 2 output channels have their output modes selected by the 16-bit User 2 Output Mode register, which is located at address 00A2h and 00A3h, and so on, up to the User 8 Output Mode register, which is found at address 00AEh and 00AFh.

Each channel has its output mode determined by two bits within the active user's Output Mode register. Bits D1 and D0 control channel 1. Bits D3 and D2 control channel 2, and so on. The bits are decoded as follows:

D3	D2	Channel 2
0	0	Output Off Low
0	1	Output Active High
1	0	Output Off High
1	1	Output Active Low

D1	D0	Channel 1
0	0	Output Off Low
0	1	Output Active High
1	0	Output Off High
1	1	Output Active Low

D7	D6	Channel 4
0	0	Output Off Low
0	1	Output Active High
1	0	Output Off High
1	1	Output Active Low

D5	D4	Channel 3
0	0	Output Off Low
0	1	Output Active High
1	0	Output Off High
1	1	Output Active Low

D11	D10	Channel 6
0	0	Output Off Low
0	1	Output Active High
1	0	Output Off High
1	1	Output Active Low

D9	D8	Channel 5
0	0	Output Off Low
0	1	Output Active High
1	0	Output Off High
1	1	Output Active Low

D15	D14	Channel 8
0	0	Output Off Low
0	1	Output Active High
1	0	Output Off High
1	1	Output Active Low

D13	D12	Channel 7
0	0	Output Off Low
0	1	Output Active High
1	0	Output Off High
1	1	Output Active Low

Under normal circumstances, the operator is free to choose any output mode. The only exception is when jumper header JP10 is left open, putting the V202 module in AGS mode.

AGS mode requires that the active outputs must be short, negative going strobes. If an output is turned off, it must remain in the high state. To ensure that these requirements are met, any channel that is programmed to output active high mode is forced to the active output low mode. Any channel that is programmed to output off low mode is forced to the output off high mode. This is done regardless of the settings in the active user's Output Mode register.

Please note that turning a channel's output off does not stop its internal triggering and timing functions. It only prevents the output pulse from appearing at the output connector. In fact, even with the output turned off, the Status register will show activity for that channel if all trigger criteria is met. To turn off all channel functions, use the Arm register.

SELECTING GATE MODE

The gate mode of a channel determines whether a pulse output is ungated, which is the normal setting, or gated. When a pulse output is ungated, the start of the pulse is determined by its own trigger and pulse delay value, and the duration of the pulse is determined by its own pulse width value. This means the duration of a pulse output is essentially indeterminate, dependent upon the time between two separate trigger events.

In gated mode, the start of the pulse is determined by the previous channel's trigger and pulse delay value, and the end of the pulse is determined by its own trigger and pulse delay value. The end of the pulse actually occurs when it programmed to go active.

Each channel within a user can be independently configured to gated or ungated mode. A different user may select different gate modes for the eight channels.

The User 1 output channels have their gate modes selected by the 8-bit User 1 Gate Mode register, which is located at address 00C1h. The User 2 output channels have their gate modes selected by the 8-bit User 2 Gate Mode register, which is located at address 00A3h, and so on, up to the User 8 Gate Mode register, which is found at address 00AFh.

Each channel has its gate mode determined by a bit within the active user's Gate Mode register. Bits D0 controls channel 1. Bit D1 control channel 2, and so on. If a bit has a value of 1, the corresponding channel is in gated mode. If a bit has a value of zero, the corresponding channel is in ungated mode.

Under normal circumstances, the operator is free to choose any gate mode. The only exception is when jumper header JP10 is left open, putting the V202 module in AGS mode.

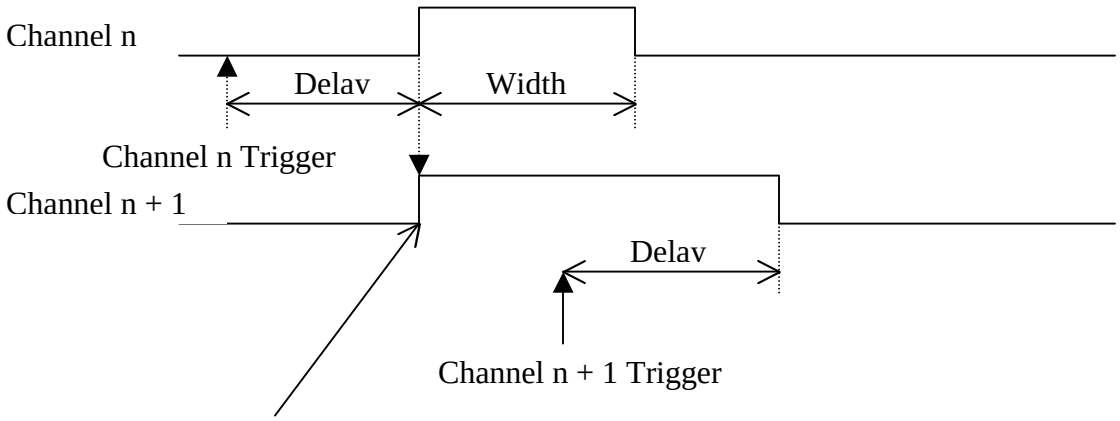
In gated mode, the duration of an active pulse is indeterminate. AGS mode requires that the active outputs must be short, negative going strobes. To ensure that these requirements are met, any channel that is programmed to gated mode is forced to the ungated mode, regardless of the settings in the active user's Gate Mode register.

If the V202 module is not in AGS mode, channel 2 through channel 7 may operate in gated mode, but channel 1 must always operate in the ungated mode. This is due to the fact that there are no channels previous to channel 1 to gate it with. Attempts to set channel 1 to the gated mode will be ignored, regardless of the value of D0 in the active user's Gate Mode register.

When a channel is configured for the gated mode, the width value that is actually loaded into that channel's width counter is forced to one, regardless of the value stored in the channel's width storage area. This means that a channel will actually go inactive one clock pulse after its pulse output goes inactive. To ensure that a value of 1 is loaded into the width counter for the first pulse, reset or arm the channel after setting it to the gated

mode. This forces the delay and width counters to be loaded (or reloaded) with the proper values.

The figure below shows an example of the gated mode.



Channel n + 1 triggers when channel n goes active

INTERRUPTS

The V202 module is capable of providing eleven different interrupts. Interrupt selection is global in nature. Any enabled interrupt is enabled across all users.

The following interrupts are available to be enabled in any combination:

1) When a parity error is seen on an Event Link word
2) When the V202 module loses lock on the Event Link (Carrier Down)
   The V202 module will not issue another Carrier Down interrupt unless a lock condition is restored, and then lost again.
3) When the V202 module regains lock on the Event Link (Carrier Up)
   The V202 module will not issue a Carrier Up interrupt unless a Carrier Down interrupt occurs first, and then lock is restored.

4-11) At the end of any one of the eight active pulse outputs

The interrupt level of the V202 module is a programmable setting, using the 8-bit Interrupt Level register at address 0021h. A value of 00h written into the register will globally disable all interrupts. A value of 01h will set the module to an interrupt level of 1. A value of 02h will set the module to an interrupt level of 2, and so on. The highest interrupt level is 7. Any data residing in the upper 5 bit positions of the register will be ignored.

The 16-bit Interrupt Vector register at address 0022h and 0023h holds the module's Status/ID word, which is presented to the VME bus by the V202 module when an interrupt is serviced. The Status/ID is set up by the operator during the initial configuration.

Each of the eleven interrupts can be individually enabled or disabled using the 16-bit Interrupt Enable register at address 002Eh and 002Fh. A "1" bit enables the corresponding interrupt. A "0" bit disables the corresponding interrupt. The enabling bits are in the same position in this register as the corresponding status bits are in the Status register. Reading the Status word will identify the active interrupt.

The interrupt events and their corresponding bits are defined below.

D15	"not used"	D7	Pulse 8 Done
D14	"not used"	D6	Pulse 7 Done
D13	Parity Error	D5	Pulse 6 Done
D12	Carrier Down	D4	Pulse 5 Done
D11	Carrier Up	D3	Pulse 4 Done
D10	"not used"	D2	Pulse 3 Done
D9	"not used"	D1	Pulse 2 Done
D8	"not used"	D0	Pulse 1 Done

A system reset will disable all interrupts by clearing the Interrupt Enable register.

SYSTEM AND PULSE RESETS

There are two ways to initiate a system reset on the V202 module. The first way is by manually resetting the entire VME crate with the reset button. The second way is to issue a system reset command from the VME controller to the V202 module's Reset register.

The Reset register is a 16-bit write-only register located at addresses 0024h and 0025h. The upper 7 bits of the high byte of this register, at address 0024h, are not used. The lowest bit of the high byte, D8, is used to implement a system reset. When a "1" is written to this bit, the V202 module will undergo a system reset. The bit will then be cleared automatically.

A system reset issued to the V202 module will do the following:

1) Synchronize output clocks
2) Clear internal control strobes
3) Clear any active interrupt
4) Restart Event Link decoder
5) Halt any active pulse outputs
6) Reload delay and width counters for all 8 channels
7) Set board to default PPM user (User 1)
8) Clear the Interrupt Enable register
9) Clear the Status register
10) Clear the User History register

In addition to a system reset, it is possible to reset the individual output channels. This will terminate the pulse output, if it is active, and cause that channel's delay and width counters to be reloaded with the appropriate values.

The eight bits of the low byte of the Reset register are used to reset the eight output channels. D0 resets channel 1. D1 resets channel 2, and so on. After a channel is reset, the corresponding reset bit will be cleared automatically.

STATUS REGISTER

There is a 16-bit read-only Status register at address 0026h and 0027h. Reading this register allows the operator to remotely observe the status of the V202 module. If interrupts are enabled, this register can tell the operator which condition caused an interrupt.

D15 is the AGS bit. A value of 1 means that the RHIC/AGS jumper header is open, and the module is in the AGS mode. (AGS mode will be discussed later in the document) D15 cannot be cleared or controlled by the operator.

D14 is the Carrier Lock bit. A value of 1 means that the V202 module's PLL is locked to the Event Link. D14 cannot be cleared or controlled by the operator.

D13 is the Parity error bit. This bit is set each time an Event Link word is received with incorrect parity. D13 is cleared automatically when the high byte of the register is read, or upon a system reset.

D12 is the Carrier Down bit. It is set once, when the V202 module has lost lock on the Event Link. It cannot reoccur unless the Event Link lock is restored, and then lost again. D12 is cleared automatically when the high byte of the register is read, or upon a system reset.

D11 is the Carrier Up bit. It is set once, when the Event Link lock has been restored. It cannot occur (or reoccur) unless the Event Link lock has first been lost. D11 is cleared automatically when the high byte of the register is read, or upon a system reset.

D10 -> D8 are the User bits. These bits show what PPM user is currently active.

000 = User 1, 001 = User 2, 010 = User 3, 011 = User 4
100 = User 5, 101 = User 6, 110 = User 7, 111 = User 8

D10 -> D8 cannot be cleared or controlled by the operator.

D7 –> D0 are the pulse activity bits. D0 is set at the end of an active pulse at pulse output 1. D1 is set at the end of an active pulse at pulse output 2, and so on. The pulse activity bits are cleared upon a system reset. The pulse activity bits are not cleared automatically when the low byte of the register is read. Instead, writing a value of 1 to a bit position within the low byte will clear that bit. Multiple bits can be cleared simultaneously. Writing a value of 0 to a bit position within the low byte will have no affect.

VME PULSE TRIGGER COMMAND

Pulse outputs are normally triggered through the Event Link look-up table. It is also possible to trigger pulse outputs with external inputs, or even other pulse outputs.

There is one other way to trigger a pulse output, and that is with a VME write transfer to the 8-bit Pulse Trigger register located at address 0017h. By setting specific bits within the register to a value of 1, the corresponding pulse outputs will be immediately triggered. D0 triggers pulse output 1, D1 triggers pulse output 2, and so on. Writing a zero to a bit will have no affect on its channel.

It is possible to trigger multiple output channels simultaneously with the same VME write command. Immediately after triggering, any bit positions in the Pulse Trigger register that were set will automatically be cleared.

There are only two requirements for this, or any other trigger method to work. These requirements must be met prior to writing to the Pulse Trigger register. First, the appropriate bits in the Pulse Arm register must be set to a value of 1 for the desired channels. Second, the Output Mode registers must be set the desired channels to either a normal or inverted output.

No matter how a channel is configured for triggering in the Trigger Mode registers, a VME trigger command will immediately trigger that channel. Even if a channel is programmed to be triggered by the start or end of a previous channel, a VME trigger will cause an immediate trigger of that channel. The normal channel delay and width times will be applied to the VME triggered pulse outputs.

If, however, a channel is configured to be a gated with a previous channel, the output of that channel will still be gated. In this case, it is recommended that the two channels do not have the same delay time if they are triggered simultaneously. Otherwise, the pulse output will be nothing more than a glitch, or perhaps not appear at all. This is due to the fact that the output register is essentially being clocked and cleared at the same time.

AGS MODE

When jumper header JP10 is left open, the V202 module operates in what is called AGS mode.
AGS mode is used specifically to allow the V202 module to interface with the "TTL to AGS Converter", through the VME backplane. The converter's onboard transistors require that the pulse outputs be short, negative going strobes.

The following conditions are fixed by the V202 module while in AGS mode, and cannot be overridden by programming:

1) The pulse width counters can only use the 1MHz or 10MHz clock. If the operator selects the external clock or the event clock, the pulse width counters will automatically use the 10MHz clock instead. The pulse delay counters will still use the clock selected by the operator.

2) The pulse width count for all channels will be forced to a value of 1. The pulse delay count remains operator selectable.

3) The gate mode will be forced to ungated.

4) The output mode will be forced to output active low, or output off high.

The registers and memory locations that control the four functions listed above will always contain the settings that the operator programmed into them. Reading these locations back on the VME bus will confirm this. However, the settings may not agree with the required operation of the V202 module when in AGS mode. In this case, the settings will be ignored.

These restrictions guarantee that all the pulse outputs in AGS mode, on the front panel as well as the backplane, will be short, negative going strobes, either 100 nanoseconds or 1 microsecond in length.

CLOCK SYNCHRONIZATION

It is possible to synchronize, or resynchronize, the V202 module's internal clocks. It is done upon the occurrence of an operator specified Event Link word. This is controlled via the 16-bit Resync Code register located at address 0028h and 0029h.

The 1MHz, 100KHz, 10KHz, and 1KHz clocks are all submultiples of the 10MHz clock, which is phase locked to the Event Link. Flip-flops are used to divide down each clock to derive the next lowest clock.

When an event happens, it may be useful to know exactly what the states of the lower frequency clocks are in relation to the 10MHz clock. After all, it takes 10,000 clocks at 10MHz to generate 1 clock period of the 1KHz clock.

To accomplish this, all the dividing flip-flops may be reset upon a specific event. From that point on it should be possible to predict when the edges of the lower clock frequencies will occur.

If D8 of the Resync Code register is set to a value of 1, the clock resynchronizing function is enabled. If D8 is zero, the clock resynchronizing function is disabled. D7->D0 is loaded with the Resync Code. The Resync Code defines the Event Link word upon whose occurrence the flip-flops will be reset, synchronizing the clocks. The flip-flops will be reset each time the Resync Code appears on the Event Link, until the clock resynchronizing function is disabled

The resynchronizing process has no affect on the 10MHz clock.

GROUNDING

There are two main ground planes on the V202 module: digital ground and earth ground. These planes are on the same layer of the board, but they are split.

The digital ground plane is used for all the onboard logic, and is very large in relation to the earth ground. Digital ground is connected to at least thirty-five backplane connector pins, distributed between P1 and P2.

The earth ground is a narrow plane that runs parallel to the front panel. Earth ground is connected to the shells of the 8 front panel pulse output connectors, and is connected to six pins on backplane connector P2C, from P2C-1 to P2C-6. If metal brackets are used to secure the front panel to the board, earth ground will be connected to the VME chassis when the module is screwed into place.

There are provisions onboard the V202 module to jumper the two main ground planes together, if so desired. This is done by shorting jumper headers JP11, JP12, and JP13. In the lab environment it has proven beneficial to configure the V202 module with the jumper headers shorted.

In addition to the two main ground planes, each of the four front panel trigger input connectors, as well as the front panel clock input connector, are positioned on their own mini-ground planes. Each of these five mini-ground planes is coupled to the earth ground through a .1-microfarad capacitor.

The shell of each input connector is connected to its mini-ground. The input signal from each connector is also referenced to its mini-ground. These signals are opto-coupled to the rest to the board's logic.

If desired, the coupling capacitor of each mini-ground can be bypassed. This connects the mini-ground directly to the earth ground. Shorting jumper header JP4 will connect the mini-ground of the TRG 1/2 connector directly to earth ground. Shorting jumper header JP5 will connect the mini-ground of the TRG 3/4 connector directly to earth ground. Shorting jumper header JP6 will connect the mini-ground of the TRG 5/6 connector directly to earth ground. Shorting jumper header JP7 will connect the mini-ground of the TRG 7/8 connector directly to earth ground. Shorting jumper header JP8 will connect the mini-ground of the CLK connector directly to earth ground.

In the lab environment it has not been necessary to short these jumper headers.

JUMPER SETTINGS

There are thirteen jumper headers on the V202 module, JP1 through JP13. All jumper headers should be in a fixed state, open or shorted, prior to applying power to the board.

JP2 is the only 3-pin jumper header. The rest of the jumper headers have two pins.

Below is a list of the jumper headers and their associated functions.

JP1 JP1 must be jumped during normal operation. It is only open when downloading firmware into U5, a programmable device that controls the PLL circuit.

JP2 JP2 selects between the Event Link input from the front panel and the Event Link input from the backplane. Jumping pins 1 and 2 enables the Event Link from the front panel. Jumping pins 2 and 3 enables the Event Link from the backplane, as long as the backplane is wired for it. Never short all three pins together. If none of the pins are jumped, the V202 will not decode the Event Link.

JP3 JP3 must be jumped during normal operation. It is only open when the PLL circuitry is being tested.

JP4 When jumped, connects the mini-ground plane of the TRG 1/2 connector to earth ground. When open, the grounds are separated.

JP5 When jumped, connects the mini-ground plane of the TRG 3/4 connector to earth ground. When open, the grounds are separated.

JP6 When jumped, connects the mini-ground plane of the TRG 5/6 connector to earth ground. When open, the grounds are separated.

JP7 When jumped, connects the mini-ground plane of the TRG 7/8 connector to earth ground. When open, the grounds are separated.

JP8 When jumped, connects the mini-ground plane of the CLK connector to earth ground. When open, the grounds are separated.

JP9 JP9 must be open during normal operation. This jumper header is a provision that would allow U36 to be replaced with an alternate device, if the SN74LS682DW part number becomes obsolete. The replacement would be an SN74ALS520DW.

JP10 JP10 is jumper for normal operation. When JP10 is open, the V202 module operates in AGS mode. See the AGS Mode section of this document for details.

JP11, JP12, JP13 These jumper headers provide a means to connect the digital ground plane to the earth ground plane. See the Grounding section of this document for details.

REVISION

This manual was written for revision C of the V202 module. It supercedes all others written before 3/10/03.

The B revision was applied the first production boards due to the prototype revision.

The C revision had three changes from revision B.

1) Changed part numbers of DS9, DS10, and DS11 from 555-0705 to 551-0609.

2) Changed part numbers of DS12 from 555-0505 to 551-0509

3) Changed EPLD software for U37 (EP1K100) and U34 (EPC2) from "94028897a.sof" and "94028897a.pof" to "94028897b.sof" and "94028897b.pof". The new software forces the V202 module into User 1 when the multiple user function is disabled. Originally, if the module had the multiple user function enabled, and then had it disabled, the module would remain in the last user.

APPENDIX A

V202 Register and Memory Assignments

Definitions

? = Lower programmable bits
$ = Upper programmable bits
X = Don't care bit
xxxxxxxx = non-existent register
Space = ASCII space character

RW = Read/Write register
RO = Read only register
WOAC = Write only, auto clear register
ROAC = Read only, auto clear register
ROWTC = Read only, write to clear register

CL = Carrier lock
CD = Carrier down
CU = Carrier up
PE = Parity error

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VME ID Registers

Address	Purpose	Access	Hi Byte	Lo Byte	
H0000	VME ID	RO	V	M	V = 56h; M = 4Dh
H0002	VME ID	RO	E	I	E = 45h: I = 49h
H0004	VME ID	RO	D	B	D = 44h: B = 42h
H0006	VME ID	RO	N	L	N = 46h: L = 4Ch
H0008	VME ID	RO	V	2	V = 56h: 2 = 32h
H000A	VME ID	RO	0	2	0 = 30h: 2 = 32h
H000C	VME ID	RO	Space	Space	Space = 20h
H000E	VME ID	RO	R	E	R = 52h: E = 45h
H0010	VME ID	RO	V	"Letter"	V = 56h; Letter = 41h---48h
H0012	VME ID	RO	Space	Space	Space = 20h
H0014	VME ID	RO	S	E	S = 53h: E = 45h
H0016	VME ID	RO	R	#	R = 52h: # = 23h
H0018	VME ID	RO	"THO"	"HUN"	THO = 30h; HUN = 30h---32h
H001A	VME ID	RO	"TEN"	"UNIT"	TEN = 30h---39h; UNIT = 30h---39h
H001C	VME ID	RO	Space	Space	Space = 20h
H001E	VME ID	RO	Space	Space	Space = 20h

Global Control Registers

Address	Purpose	Access	Hi Byte	Lo Byte	
H0020	INT LEVEL	RW	xxxxxxxx	XXXXX ???	A value of 000 will disable interrupt
H0022	INT VECTOR	RW	$$$$$$$$	????????	Status/ID interrupt response
H0024	SYS & PULSE RST	WOAC	XXXXXXX $	????????	$ = Sys rst; ? = Rst Ch 8,7,6,5,4,3,2,1
H0026	STATUS	ROAC; ROWTC	$$$$$$$$	????????	$=AGS,CL,PE,CD,CU,USR 2..0; ? = End of pulse 8,7,6,5,4,3,2,1
H0028	RESYNC CODE	RW	XXXXXXX $	????????	$ = 1 = Resync active; ???????? = Resync event Code
H002A	PULSE ARM	RW	xxxxxxxx	????????	? = Arm Pulse 8,7,6,5,4,3,2,1
H002C	PULSE TRIGGER	WOAC	xxxxxxxx	????????	? = Trigger Pulse 8,7,6,5,4,3,2,1
H002E	INT ENABLE	RW	XX $$$ XXX	????????	1 = Int enabled ; See Status Reg

User Control Registers

Address	Purpose	Access	Hi Byte	Lo Byte	
H0040	USER SWITCH	RW	XXXXXXX $	????????	$ = 1 = PPM active; ? = Switch event code
H0042	USER 1 CODE	RW	XXXXXXX $	????????	$ = 1 = User 1 on; ? = User 1 event code
H0044	USER 2 CODE	RW	XXXXXXX $	????????	$ = 1 = User 2 on; ? = User 2 event code
H0046	USER 3 CODE	RW	XXXXXXX $	????????	$ = 1 = User 3 on; ? = User 3 event code
H0048	USER 4 CODE	RW	XXXXXXX $	????????	$ = 1 = User 4 on; ? = User 4 event code
H004A	USER 5 CODE	RW	XXXXXXX $	????????	$ = 1 = User 5 on; ? = User 5 event code
H004C	USER 6 CODE	RW	XXXXXXX $	????????	$ = 1 = User 6 on; ? = User 6 event code
H004E	USER 7 CODE	RW	XXXXXXX $	????????	$ = 1 = User 7 on; ? = User 7 event code
H0050	USER 8 CODE	RW	XXXXXXX $	????????	$ = 1 = User 8 on; ? = User 8 event code
H0052	USER HISTORY	ROWTC	xxxxxxxx	????????	$ = User 8..1 was active

Clock Mode Registers

Address	Purpose	Access	Hi Byte	Lo Byte	
			C8 C7 C6 C5	C4 C3 C2 C1	00=10MHz; 01=1MHz; 10=Ext Clk; 11=Event Clk
H0060	USER 1 CLK MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H0062	USER 2 CLK MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel1; C2 = Channel 2: etc
H0064	USER 3 CLK MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H0066	USER 4 CLK MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H0068	USER 5 CLK MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H006A	USER 6 CLK MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H006C	USER 7 CLK MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H006E	USER 8 CLK MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc

Clock Event Registers

Address	Purpose	Access	Hi Byte	Lo Byte	
H0070	USER 1 CLK EVENT	RW	xxxxxxxx	????????	???????? = Event clock code
H0072	USER 2 CLK EVENT	RW	xxxxxxxx	????????	???????? = Event clock code
H0074	USER 3 CLK EVENT	RW	xxxxxxxx	????????	???????? = Event clock code
H0076	USER 4 CLK EVENT	RW	xxxxxxxx	????????	???????? = Event clock code
H0078	USER 5 CLK EVENT	RW	xxxxxxxx	????????	???????? = Event clock code
H007A	USER 6 CLK EVENT	RW	xxxxxxxx	????????	???????? = Event clock code
H007C	USER 7 CLK EVENT	RW	xxxxxxxx	????????	???????? = Event clock code
H007E	USER 8 CLK EVENT	RW	xxxxxxxx	????????	???????? = Event clock code

Trigger Mode Registers

Address	Purpose	Access	Hi Byte	Lo Byte	
			C8 C7 C6 C5	C4 C3 C2 C1	00=Timeline; 01=External; 10=Previous chan start;
H0080	USER 1 TRIG MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	11=Previous chan end
H0082	USER 2 TRIG MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H0084	USER 3 TRIG MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H0086	USER 4 TRIG MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H0088	USER 5 TRIG MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H008A	USER 6 TRIG MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H008C	USER 7 TRIG MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H008E	USER 8 TRIG MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc

Output Mode Registers

Address	Purpose	Access	Hi Byte	Lo Byte	
					00=Output off lo; 01=Output active hi
			C8 C7 C6 C5	C4 C3 C2 C1	10=Output off hi; 11=Output active lo
H00A0	USR 1 OUTPUT MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H00A2	USR 2 OUTPUT MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H00A4	USR 3 OUTPUT MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H00A6	USR 4 OUTPUT MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H00A8	USR 5 OUTPUT MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H00AA	USR 6 OUTPUT MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H00AC	USR 7 OUTPUT MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc
H00AE	USR 8 OUTPUT MODE	RW	$$ $$ $$ $$	?? ?? ?? ??	C1 = Channel 1; C2 = Channel 2: etc

Gate Mode Registers

Address	Purpose	Access	Hi Byte	Lo Byte	
				C8 - C1	0 = Ungated mode; 1 = Gated mode
H00C0	USER 1 GATE MODE	RW	xxxxxxxx	????????	C1 = Channel 1; C2 = Channel 2: etc
H00C2	USER 2 GATE MODE	RW	xxxxxxxx	????????	C1 = Channel 1; C2 = Channel 2: etc
H00C4	USER 3 GATE MODE	RW	xxxxxxxx	????????	C1 = Channel 1; C2 = Channel 2: etc
H00C6	USER 4 GATE MODE	RW	xxxxxxxx	????????	C1 = Channel 1; C2 = Channel 2: etc
H00C8	USER 5 GATE MODE	RW	xxxxxxxx	????????	C1 = Channel 1; C2 = Channel 2: etc
H00CA	USER 6 GATE MODE	RW	xxxxxxxx	????????	C1 = Channel 1; C2 = Channel 2: etc
H00CC	USER 7 GATE MODE	RW	xxxxxxxx	????????	C1 = Channel 1; C2 = Channel 2: etc
H00CE	USER 8 GATE MODE	RW	xxxxxxxx	????????	C1 = Channel 1; C2 = Channel 2: etc

Channel 1 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0200	CH1 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0202	CH1 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0204	CH1 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0206	CH1 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0208	CH1 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H020A	CH1 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H020C	CH1 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H020E	CH1 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0210	CH1 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0212	CH1 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0214	CH1 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0216	CH1 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0218	CH1 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H021A	CH1 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H021C	CH1 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H021E	CH1 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0220	CH1 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0222	CH1 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0224	CH1 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0226	CH1 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0228	CH1 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H022A	CH1 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H022C	CH1 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H022E	CH1 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0230	CH1 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0232	CH1 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0234	CH1 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0236	CH1 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0238	CH1 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H023A	CH1 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H023C	CH1 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H023E	CH1 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 1 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0240	CH1 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0242	CH1 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0244	CH1 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0246	CH1 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0248	CH1 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H024A	CH1 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H024C	CH1 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H024E	CH1 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0250	CH1 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0252	CH1 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0254	CH1 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0256	CH1 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0258	CH1 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H025A	CH1 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H025C	CH1 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H025E	CH1 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0260	CH1 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0262	CH1 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0264	CH1 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0266	CH1 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0268	CH1 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H026A	CH1 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H026C	CH1 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H026E	CH1 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0270	CH1 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0272	CH1 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0274	CH1 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0276	CH1 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0278	CH1 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H027A	CH1 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H027C	CH1 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H027E	CH1 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 2 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0280	CH2 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0282	CH2 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0284	CH2 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0286	CH2 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0288	CH2 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H028A	CH2 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H028C	CH2 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H028E	CH2 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0290	CH2 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0292	CH2 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0294	CH2 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0296	CH2 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0298	CH2 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H029A	CH2 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H029C	CH2 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H029E	CH2 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H02A0	CH2 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H02A2	CH2 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H02A4	CH2 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H02A6	CH2 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H02A8	CH2 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H02AA	CH2 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H02AC	CH2 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H02AE	CH2 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H02B0	CH2 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H02B2	CH2 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H02B4	CH2 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H02B6	CH2 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H02B8	CH2 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H02BA	CH2 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H02BC	CH2 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H02BE	CH2 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 2 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H02C0	CH2 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H02C2	CH2 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H02C4	CH2 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H02C6	CH2 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H02C8	CH2 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H02CA	CH2 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H02CC	CH2 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H02CE	CH2 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H02D0	CH2 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H02D2	CH2 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H02D4	CH2 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H02D6	CH2 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H02D8	CH2 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H02DA	CH2 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H02DC	CH2 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H02DE	CH2 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H02E0	CH2 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H02E2	CH2 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H02E4	CH2 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H02E6	CH2 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H02E8	CH2 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H02EA	CH2 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H02EC	CH2 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H02EE	CH2 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H02F0	CH2 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H02F2	CH2 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H02F4	CH2 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H02F6	CH2 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H02F8	CH2 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H02FA	CH2 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H02FC	CH2 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H02FE	CH2 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 3 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0300	CH3 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0302	CH3 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0304	CH3 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0306	CH3 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0308	CH3 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H030A	CH3 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H030C	CH3 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H030E	CH3 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0310	CH3 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0312	CH3 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0314	CH3 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0316	CH3 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0318	CH3 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H031A	CH3 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H031C	CH3 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H031E	CH3 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0320	CH3 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0322	CH3 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0324	CH3 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0326	CH3 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0328	CH3 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H032A	CH3 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H032C	CH3 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H032E	CH3 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0330	CH3 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0332	CH3 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0334	CH3 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0336	CH3 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0338	CH3 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H033A	CH3 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H033C	CH3 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H033E	CH3 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 3 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0340	CH3 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0342	CH3 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0344	CH3 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0346	CH3 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0348	CH3 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H034A	CH3 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H034C	CH3 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H034E	CH3 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0350	CH3 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0352	CH3 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0354	CH3 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0356	CH3 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0358	CH3 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H035A	CH3 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H035C	CH3 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H035E	CH3 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0360	CH3 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0362	CH3 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0364	CH3 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0366	CH3 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0368	CH3 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H036A	CH3 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H036C	CH3 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H036E	CH3 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0370	CH3 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0372	CH3 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0374	CH3 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0376	CH3 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0378	CH3 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H037A	CH3 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H037C	CH3 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H037E	CH3 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 4 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0380	CH4 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0382	CH4 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0384	CH4 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0386	CH4 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0388	CH4 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H038A	CH4 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H038C	CH4 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H038E	CH4 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0390	CH4 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0392	CH4 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0394	CH4 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0396	CH4 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0398	CH4 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H039A	CH4 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H039C	CH4 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H039E	CH4 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H03A0	CH4 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H03A2	CH4 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H03A4	CH4 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H03A6	CH4 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H03A8	CH4 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H03AA	CH4 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H03AC	CH4 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H03AE	CH4 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H03B0	CH4 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H03B2	CH4 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H03B4	CH4 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H03B6	CH4 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H03B8	CH4 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H03BA	CH4 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H03BC	CH4 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H03BE	CH4 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 4 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H03C0	CH4 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H03C2	CH4 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H03C4	CH4 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H03C6	CH4 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H03C8	CH4 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H03CA	CH4 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H03CC	CH4 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H03CE	CH4 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H03D0	CH4 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H03D2	CH4 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H03D4	CH4 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H03D6	CH4 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H03D8	CH4 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H03DA	CH4 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H03DC	CH4 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H03DE	CH4 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H03E0	CH4 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H03E2	CH4 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H03E4	CH4 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H03E6	CH4 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H03E8	CH4 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H03EA	CH4 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H03EC	CH4 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H03EE	CH4 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H03F0	CH4 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H03F2	CH4 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H03F4	CH4 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H03F6	CH4 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H03F8	CH4 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H03FA	CH4 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H03FC	CH4 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H03FE	CH4 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 5 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0400	CH5 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0402	CH5 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0404	CH5 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0406	CH5 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0408	CH5 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H040A	CH5 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H040C	CH5 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H040E	CH5 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0410	CH5 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0412	CH5 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0414	CH5 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0416	CH5 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0418	CH5 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H041A	CH5 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H041C	CH5 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H041E	CH5 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0420	CH5 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0422	CH5 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0424	CH5 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0426	CH5 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0428	CH5 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H042A	CH5 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H042C	CH5 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H042E	CH5 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0430	CH5 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0432	CH5 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0434	CH5 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0436	CH5 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0438	CH5 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H043A	CH5 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H043C	CH5 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H043E	CH5 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 5 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0440	CH5 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0442	CH5 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0444	CH5 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0446	CH5 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0448	CH5 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H044A	CH5 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H044C	CH5 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H044E	CH5 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0450	CH5 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0452	CH5 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0454	CH5 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0456	CH5 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0458	CH5 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H045A	CH5 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H045C	CH5 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H045E	CH5 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0460	CH5 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0462	CH5 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0464	CH5 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0466	CH5 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0468	CH5 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H046A	CH5 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H046C	CH5 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H046E	CH5 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0470	CH5 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0472	CH5 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0474	CH5 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0476	CH5 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0478	CH5 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H047A	CH5 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H047C	CH5 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H047E	CH5 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 6 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0480	CH6 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0482	CH6 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0484	CH6 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0486	CH6 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0488	CH6 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H048A	CH6 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H048C	CH6 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H048E	CH6 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0490	CH6 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0492	CH6 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0494	CH6 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0496	CH6 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0498	CH6 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H049A	CH6 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H049C	CH6 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H049E	CH6 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H04A0	CH6 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H04A2	CH6 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H04A4	CH6 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H04A6	CH6 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H04A8	CH6 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H04AA	CH6 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H04AC	CH6 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H04AE	CH6 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H04B0	CH6 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H04B2	CH6 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H04B4	CH6 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H04B6	CH6 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H04B8	CH6 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H04BA	CH6 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H04BC	CH6 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H04BE	CH6 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 6 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H04C0	CH6 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H04C2	CH6 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H04C4	CH6 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H04C6	CH6 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H04C8	CH6 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H04CA	CH6 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H04CC	CH6 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H04CE	CH6 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H04D0	CH6 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H04D2	CH6 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H04D4	CH6 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H04D6	CH6 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H04D8	CH6 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H04DA	CH6 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H04DC	CH6 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H04DE	CH6 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H04E0	CH6 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H04E2	CH6 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H04E4	CH6 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H04E6	CH6 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H04E8	CH6 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H04EA	CH6 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H04EC	CH6 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H04EE	CH6 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H04F0	CH6 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H04F2	CH6 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H04F4	CH6 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H04F6	CH6 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H04F8	CH6 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H04FA	CH6 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H04FC	CH6 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H04FE	CH6 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 7 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0500	CH7 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0502	CH7 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0504	CH7 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0506	CH7 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0508	CH7 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H050A	CH7 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H050C	CH7 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H050E	CH7 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0510	CH7 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0512	CH7 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0514	CH7 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0516	CH7 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0518	CH7 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H051A	CH7 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H051C	CH7 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H051E	CH7 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0520	CH7 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0522	CH7 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0524	CH7 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0526	CH7 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0528	CH7 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H052A	CH7 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H052C	CH7 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H052E	CH7 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0530	CH7 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0532	CH7 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0534	CH7 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0536	CH7 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0538	CH7 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H053A	CH7 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H053C	CH7 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H053E	CH7 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 7 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0540	CH7 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0542	CH7 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0544	CH7 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0546	CH7 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0548	CH7 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H054A	CH7 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H054C	CH7 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H054E	CH7 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0550	CH7 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0552	CH7 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0554	CH7 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0556	CH7 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0558	CH7 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H055A	CH7 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H055C	CH7 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H055E	CH7 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0560	CH7 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0562	CH7 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0564	CH7 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0566	CH7 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0568	CH7 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H056A	CH7 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H056C	CH7 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H056E	CH7 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0570	CH7 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0572	CH7 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0574	CH7 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0576	CH7 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0578	CH7 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H057A	CH7 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H057C	CH7 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H057E	CH7 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 8 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H0580	CH8 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0582	CH8 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0584	CH8 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0586	CH8 USER 1 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0588	CH8 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H058A	CH8 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H058C	CH8 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H058E	CH8 USER 1 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H0590	CH8 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H0592	CH8 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H0594	CH8 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H0596	CH8 USER 2 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H0598	CH8 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H059A	CH8 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H059C	CH8 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H059E	CH8 USER 2 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H05A0	CH8 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H05A2	CH8 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H05A4	CH8 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H05A6	CH8 USER 3 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H05A8	CH8 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H05AA	CH8 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H05AC	CH8 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H05AE	CH8 USER 3 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H05B0	CH8 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H05B2	CH8 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H05B4	CH8 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H05B6	CH8 USER 4 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H05B8	CH8 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H05BA	CH8 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H05BC	CH8 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H05BE	CH8 USER 4 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Channel 8 Delay And Width Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
H05C0	CH8 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H05C2	CH8 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H05C4	CH8 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H05C6	CH8 USER 5 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H05C8	CH8 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H05CA	CH8 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H05CC	CH8 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H05CE	CH8 USER 5 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H05D0	CH8 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H05D2	CH8 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H05D4	CH8 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H05D6	CH8 USER 6 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H05D8	CH8 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H05DA	CH8 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H05DC	CH8 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H05DE	CH8 USER 6 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H05E0	CH8 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H05E2	CH8 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H05E4	CH8 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H05E6	CH8 USER 7 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H05E8	CH8 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H05EA	CH8 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H05EC	CH8 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H05EE	CH8 USER 7 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0
H05F0	CH8 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 31-24
H05F2	CH8 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 23-16
H05F4	CH8 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 15-8
H05F6	CH8 USER 8 DELAY	RW	xxxxxxxx	????????	???????? = Delay bits 7-0
H05F8	CH8 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 31-24
H05FA	CH8 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 23-16
H05FC	CH8 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 15-8
H05FE	CH8 USER 8 WIDTH	RW	xxxxxxxx	????????	???????? = Width bits 7-0

Event Link Look-Up Table External Memory

Address	Purpose	Access	Hi Byte	Lo Byte	
				C8 - C1	
H1000	User 1 Table	RW	xxxxxxxx	????????	256 bytes; Each bit represents a channel
:	:	RW	xxxxxxxx	????????	D0 = CH1; D1 = CH2; D2 = CH3; D3 = CH4
H11FF	:	RW	xxxxxxxx	????????	D4 = CH5; D5 = CH6; D6 = CH7; D7 = CH8

Address	Purpose	Access	Hi Byte	Lo Byte	
H1200	User 2 Table	RW	xxxxxxxx	????????	256 bytes; Each bit represents a channel
:	:	RW	xxxxxxxx	????????	D0 = CH1; D1 = CH2; D2 = CH3; D3 = CH4
H13FF	:	RW	xxxxxxxx	????????	D4 = CH5; D5 = CH6; D6 = CH7; D7 = CH8

Address	Purpose	Access	Hi Byte	Lo Byte	
H1400	User 3 Table	RW	xxxxxxxx	????????	256 bytes; Each bit represents a channel
:	:	RW	xxxxxxxx	????????	D0 = CH1; D1 = CH2; D2 = CH3; D3 = CH4
H15FF	:	RW	xxxxxxxx	????????	D4 = CH5; D5 = CH6; D6 = CH7; D7 = CH8

Address	Purpose	Access	Hi Byte	Lo Byte	
H1600	User 4 Table	RW	xxxxxxxx	????????	256 bytes; Each bit represents a channel
:	:	RW	xxxxxxxx	????????	D0 = CH1; D1 = CH2; D2 = CH3; D3 = CH4
H17FF	:	RW	xxxxxxxx	????????	D4 = CH5; D5 = CH6; D6 = CH7; D7 = CH8

Address	Purpose	Access	Hi Byte	Lo Byte	
H1800	User 5 Table	RW	xxxxxxxx	????????	256 bytes; Each bit represents a channel
:	:	RW	xxxxxxxx	????????	D0 = CH1; D1 = CH2; D2 = CH3; D3 = CH4
H19FF	:	RW	xxxxxxxx	????????	D4 = CH5; D5 = CH6; D6 = CH7; D7 = CH8

Address	Purpose	Access	Hi Byte	Lo Byte	
H1A00	User 6 Table	RW	xxxxxxxx	????????	256 bytes; Each bit represents a channel
:	:	RW	xxxxxxxx	????????	D0 = CH1; D1 = CH2; D2 = CH3; D3 = CH4
H1BFF	:	RW	xxxxxxxx	????????	D4 = CH5; D5 = CH6; D6 = CH7; D7 = CH8

Address	Purpose	Access	Hi Byte	Lo Byte	
H1C00	User 7 Table	RW	xxxxxxxx	????????	256 bytes; Each bit represents a channel
:	:	RW	xxxxxxxx	????????	D0 = CH1; D1 = CH2; D2 = CH3; D3 = CH4
H1DFF	:	RW	xxxxxxxx	????????	D4 = CH5; D5 = CH6; D6 = CH7; D7 = CH8

Address	Purpose	Access	Hi Byte	Lo Byte	
H1E00	User 8 Table	RW	xxxxxxxx	????????	256 bytes; Each bit represents a channel
:	:	RW	xxxxxxxx	????????	D0 = CH1; D1 = CH2; D2 = CH3; D3 = CH4
H1FFF	:	RW	xxxxxxxx	????????	D4 = CH5; D5 = CH6; D6 = CH7; D7 = CH8

APPENDIX B

V202 Register and Memory Descriptions

The bit positions of all 16-bit registers are referenced as follows:

MSB—D15.D14.D13.D12.D11.D10.D9.D8 D7.D6.D5.D4.D3.D2.D1.D0—LSB
High Byte Low Byte

Table Of Contents

VME ID Registers (Address 0000h -> 001Fh)

Purpose: These sixteen consecutive registers hold the module's VME ID message.

These are 16-bit read-only registers. They reside in the area from 0000h to 001Fh. The contents of these registers are ASCII representations. They identify the type, rev, and serial number of the module. Starting at address 0000h, the VME ID should read as follows:

VMEIDBNLV202(sp)(sp)REVx(sp)(sp)SER#xxxx(sp)(sp)(sp)(sp)

* (sp) is the ASCII space character, 20h

Global Control Registers (Address 0021h -> 002Fh)

Interrupt Level Register (Address: 0021h)

Purpose: Enables interrupts globally when programmed with the module's interrupt level. Must be programmed by operator.

This is an 8-bit read-write register, used to set the interrupt level of the module. Only the lowest 3 bits (D2, D1, D0) of the register are used. The high byte at VME address 0020h doesn't actually exist. If an attempt is made to read the high byte, the value returned will be indeterminate.

A value of 00h written into the Interrupt Level register will globally disable all interrupt functions. The other valid values are 01h through 07h. Any of these values will globally enable the interrupt function.

Interrupt Vector Register (Address 0022h -> 0023h)

Purpose: Holds the Interrupt Status/ID word returned by the module when its interrupt is serviced. Must be programmed by operator.

This is a 16-bit read-write register that holds the Interrupt STATUS/ID word. This word is placed on the VME bus by the V202 module when its interrupt is being serviced.

System & Pulse Reset Register (Address 0024h -> 0025h)

Purpose: Provides the means to reset the module. Also provides the means to reset individual channels.

This is a 16-bit write-only register. The upper 7 bits of the high byte of this register are not used. The lowest bit of the high byte (D8) is for a system reset. When a "1" is written to this bit, a system reset will occur. The bit will then be cleared automatically.

A system reset will do the following:

1) Synchronize output clocks
2) Clear internal control strobes
3) Clear any active interrupt
4) Restart Event Link decoder
5) Halt any active pulse outputs
6) Reload delay and width counters for all 8 channels
7) Set board to default PPM user (User 1)
8) Clear the Interrupt Enable register
9) Clear the Status register
10) Clear the User History Register

The 8 bits of the low byte are used to clear, or reset, an active pulse output. Writing a "1" to D0 resets Pulse 1. Writing a "1" to D1 resets Pulse 2, and so on. After a pulse output is reset, the corresponding bit will be cleared automatically.

Status Register (Address 0026h -> 0027h)

Purpose: Holds the status of the V202 module. If interrupts are enabled, this register can tell the operator which condition caused an interrupt.

This is a 16-bit read-only register.

D15 is the AGS bit. A value of 1 means that the RHIC/AGS jumper header is open, and the module is in the AGS mode. D15 cannot be cleared or controlled by the operator.

D14 is the Carrier Lock bit. A value of 1 means that the V202 module's PLL is locked to the Event Link. D14 cannot be cleared or controlled by the operator.

D13 is the Parity error bit. This bit is set each time an Event Link word is received with incorrect parity. D13 is cleared automatically when the high byte of the register is read, or upon a system reset.

D12 is the Carrier Down bit. It is set once, when the V202 module has lost lock on the Event Link. It cannot reoccur unless the Event Link lock is restored, and then lost again. D12 is cleared automatically when the high byte of the register is read, or upon a system reset.

D11 is the Carrier Up bit. It is set once, when the Event Link lock has been restored. It cannot occur (or reoccur) unless the Event Link lock has first been lost. D11 is cleared automatically when the high byte of the register is read, or upon a system reset.

D10 -> D8 are the User bits. These bits show what PPM user is currently active.

000 = User 1, 001 = User 2, 010 = User 3, 011 = User 4
100 = User 5, 101 = User 6, 110 = User 7, 111 = User 8

D10 -> D8 cannot be cleared or controlled by the operator.

D7 –> D0 are the pulse activity bits. D0 is set at the end of an active pulse at pulse output 1. D1 is set at the end of an active pulse at pulse output 2, and so on. The pulse activity bits are cleared upon a system reset. The pulse activity bits are not cleared automatically when the low byte of the register is read. Instead, writing a value of 1 to a bit position within the low byte will clear that bit. Multiple bits can be cleared simultaneously. Writing a value of 0 to a bit position within the low byte will have no affect.

Resync Code Register (Address 0028h -> 0029h)

Purpose: Allows the operator to set-up the V202 module so that it synchronizes its internal clocks upon each occurrence of a specified Event Link word.

This is a 16-bit read-write register. Only the last bit of the high byte (D8) is used. All 8 bits of the low byte are functional.

Onboard the V202 module there are sub multiple clocks (1MHz, 100KHz, 10KHz, and 1KHz) generated from the 10MHz Event Link clock. To "resync" the clocks, an Event Link word is defined in the Resync Code register. When this word occurs on the Event Link, and the Resync Active bit is set, the clocks are "synchronized".

D8 is the Resync Active bit. When this bit is set, the V202 module looks for an Event Link Resync word. If this bit is "0", the Resync function is disabled.

D7 –> D0 defines the Event Link word that will resynchronize the clocks.

Pulse Arm Register (Address 002Bh)

Purpose: Globally arms each channel. Must be programmed by the operator.

NOTE! This should be the last register set-up by the operator.

This is an 8-bit read-write register used to arm the pulse outputs. A pulse output cannot be generated unless it is first armed. The high byte at VME address 002Ah doesn't actually exist. If an attempt is made to read this address location, the value returned will be indeterminate.

Each pulse output is individually armed by a bit in the Pulse Arm register. Setting D0 arms pulse 1, setting D1 arms pulse 2, and so on. Clearing a bit disables the corresponding pulse output. Multiple pulse outputs can be armed or disarmed simultaneously.

Pulse Trigger Register (Address 002Dh)

Purpose: Provides the means to trigger any of the pulse outputs with a VME write transfer.

This is an 8-bit write-only register with automatic clear that gives the VME controller the ability to trigger an output pulse on command. The high byte at VME address 002Ch doesn't actually exist. If an attempt is made to read this address location, the value returned will be indeterminate.

Each pulse output is individually triggered by a corresponding bit in the Pulse Trigger register. Setting D0 triggers pulse 1, setting D1 triggers pulse 2, and so on. Triggering occurs immediately, regardless of the configuration of the Trigger Mode register. Multiple pulse outputs may be triggered simultaneously. Once a pulse output has been triggered, its Pulse Trigger bit is automatically cleared.

The pulse outputs can only be triggered if they are first armed in the Pulse Arm register. It should be noted that when a pulse output is triggered, the pulse itself will not appear until after the programmed pulse delay has expired. Likewise, the length of the pulse is still controlled by the programmed pulse width.

Interrupt Enable Register (Address 002Eh -> 002Fh)

Purpose: Enables any or all of the eleven interrupts individually. Must be programmed by operator.

This is a 16-bit read-write register that holds the individual Interrupt Enable bits. A "1" bit enables the corresponding interrupt. A "0" bit disables the corresponding interrupt.

The interrupt level setting in the Interrupt Level register must be set to a value of 1 -> 7 to globally enable interrupts. If the Interrupt Level register contains zero, all interrupts are disabled.

To determine which event has caused an interrupt, the operator must read the Status register. The enabling bits of the Interrupt Enable register are in the same position as the corresponding status bits in the Status register. The interrupt events and their bits are defined below

D15	"not used"	D7	Pulse 8 Done
D14	"not used"	D6	Pulse 7 Done
D13	Parity Error	D5	Pulse 6 Done
D12	Carrier Down	D4	Pulse 5 Done
D11	Carrier Up	D3	Pulse 4 Done
D10	"not used"	D2	Pulse 3 Done
D9	"not used"	D1	Pulse 2 Done
D8	"not used"	D0	Pulse 1 Done

A system reset will disable all interrupts by clearing the Interrupt Enable register.

User Control Registers (Address 0040h -> 0053h)

User Switch Register (Address 0040h -> 0041h)

Purpose: Allows the operator to set-up the V202 module in PPM mode. Users will switch upon each occurrence of a specified Event Link word, assuming a valid user code has occurred first.

This is a 16-bit read-write register. Only the last bit of the high byte (D8) is used. All 8 bits of the low byte are functional.

D8 is the PPM Mode Active bit. When this bit is set, the V202 module can be programmed with multiple users. If this bit is "0", the multiple user function is disabled, putting the V202 module in the non-PPM mode. When the multiple user function is disabled, the User Code registers are ignored, and all programmable parameters must be set-up in the User 1 registers.

D7 –> D0 defines the User Switch Code. This is the Event Link word that will cause the V202 to switch to the next user. Normally this would be an event such as Pre-Pulse, or T0. The next user is predetermined by an Event Link occurrence of a pre-programmed User Code.

If two or more User Codes appear prior to the User Switch Code, the latest one will determine which user to switch to. If a User Code appears while the V202 Module is already in that user, it will be ignored.

User 1 Code Register (Address 0042h -> 0043h)

Purpose: Allows the operator to select the Event Link word that defines User 1.

This is a 16-bit read-write register. Only the last bit of the high byte (D8) is used. All 8 bits of the low byte are functional.

D8 is the User 1 Active bit. When this bit is set, the V202 module will look for the occurrence of the User 1 Code on the Event Link. When this word is seen, the next occurrence of the User Switch Code will cause the V202 module to switch to User 1. When this bit is "0", User 1 will not be an active user.

D7 –> D0 defines the User 1 Code. It is the Event Link word that prepares the V202 module to switch to User 1. The actual switch occurs on the Event Link occurrence of the User Switch Code.

It is recommended when using PPM mode that User 1 always be enabled. User 1 is the default user, and is the active user upon power-up and system resets.

User 2 Code Register (Address 0044h -> 0045h)

Purpose: Allows the operator to select the Event Link word that defines User 2.

This is a 16-bit read-write register. Only the last bit of the high byte (D8) is used. All 8 bits of the low byte are functional.

D8 is the User 2 Active bit. When this bit is set, the V202 module will look for the occurrence of the User 2 Code on the Event Link. When this word is seen, the next occurrence of the User Switch Code will cause the V202 module to switch to User 2. When this bit is "0", User 2 will not be an active user.

D7 –> D0 defines the User 2 Code. It is the Event Link word that prepares the V202 module to switch to User 2. The actual switch occurs on the Event Link occurrence of the User Switch Code.

User 3 -> User 8 Code Registers (Address 0046h -> 0051h)

Purpose: Allows the operator to select the Event Link words that defines User 3 through User 8.

The User 3 through User 8 Code registers operate the same as the User 2 Code register.

User History Register (Address 0053h)

Purpose: Contains a history of users that have been active.

This is an 8-bit read-only, write-to-clear register. Each bit of this register represents a user. D0 represents User 1, D1 represents User 2, and so on. Whenever a user is activated, its corresponding bit in the User History register is set to a value of 1. If a user is never activated its bit remains at zero.

The History register is not cleared with a system reset. Nor is it cleared automatically when the register is read. Instead, writing a value of 1 to a bit position within the register clears that bit. Multiple bits can be cleared simultaneously. Writing a value of 0 to a bit position will have no affect on the register.

Clock Mode Registers (Address 0060h -> 006Fh)

Each user within the V202 module can have its channels individually programmed to accept one of four clock sources:

1) 10 MHz clock
2) 1 MHz clock
3) External clock (up to 5 MHz)
4) Event code clock. This is a clock that pulses each time a predefined word appears on the Event Link.

User 1 Clock Mode Register (Address 0060h -> 0061h)

Purpose: Allows the operator to select the clock mode for each of the eight channels while the V202 module is in User 1, or while the V202 module is in non-PPM mode.

This is a 16-bit read-write register. Each channel has its clock mode determined by two bits within the User 1 Clock Mode register. Bits D0 and D1 control channel 1. Bits D2 and D3 control channel 2, and so on.

The following bit pairs and their codes determine which clock will be used for the delay and width counters of each channel:

D1	D0		Channel 1
D3	D2		Channel 2
D5	D4		Channel 3
D7	D6		Channel 4
D9	D8		Channel 5
D11	D10		Channel 6
D13	D12		Channel 7
D15	D16		Channel 1
0	0	=	10MHz
0	1	=	1MHz
1	0	=	External
1	1	=	Event code

User 2 Clock Mode Register (Address 0062h -> 0063h)

Purpose: Allows the operator to select the clock mode for each of the eight channels while the V202 module is in User 2.

This is a 16-bit read-write register. Each channel has its clock mode determined by two bits within the User 2 Clock Mode register. Bits D0 and D1 control channel 1. Bits D2 and D3 control channel 2, and so on.

The following bit pairs and their codes determine which clock will be used for the delay and width counters of each channel:

D1	D0		Channel 1
D3	D2		Channel 2
D5	D4		Channel 3
D7	D6		Channel 4
D9	D8		Channel 5
D11	D10		Channel 6
D13	D12		Channel 7
D15	D16		Channel 1
0	0	=	10MHz
0	1	=	1MHz
1	0	=	External
1	1	=	Event code

User 3 -> User 8 Clock Mode Registers (Address 0064h -> 006Fh)

Purpose: Allows the operator to select the clock mode for each of the eight channels within User 3 through User 8.

The User 3 through User 8 Clock Mode registers operate the same as the User 2 Clock Mode register.

Clock Event Registers (Address 0071h -> 007Fh)

An event clock pulse occurs each time a predefined Clock Event Code appears on the Event Link. This pulse can be used to clock the delay and width counters of each channel.

If a Clock Event Code is the same as the User Switch Code, no pulse will be generated when a user change occurs. However, it is possible for a user change not occur when a User Switch Code appears. In this case, an event clock pulse would be generated.

All eight channels within a user use the same Clock Event Code. However, the Clock Event Code may change from user to user.

User 1 Clock Event Register (VME: 0071h)

Purpose: Allows the operator to define the Event Link work whose occurrence will generate an event clock pulse while the V202 module is in User 1, or while the V202 module is in non-PPM mode.

This is an 8-bit read-write register. The high byte at VME address 0070h doesn't actually exist. If an attempt is made to read these bit locations, the value returned will be indeterminate.

D7 –> D0 defines the User 1 Clock Event. It is the Event Link word that will cause a pulse to be generated while the V202 module is in User 1, or while the V202 module is in non-PPM mode.

User 2 Clock Event Register (VME: 0073h)

Purpose: Allows the operator to define the Event Link work whose occurrence will generate an event clock pulse while the V202 module is in User 2.

This is an 8-bit read-write register. The high byte at VME address 0072h doesn't actually exist. If an attempt is made to read these bit locations, the value returned will be indeterminate.

D7 –> D0 defines the User 2 Clock Event. It is the Event Link word that will cause a pulse to be generated while the V202 module is in User 2.

User 3 -> User 8 Clock Event Registers (Address 0075h -> 007Fh)

Purpose: Allows the operator to select the clock event for each of the eight channels within User 3 through User 8.

The User 3 through User 8 Clock Event registers operate the same as the User 2 Clock Event register.

Trigger Mode Registers (Address 0080h -> 008Fh)

A pulse output can be triggered in one of four ways:

1) Event Link word
2) External input
3) Start of previous channel pulse
4) End of previous channel pulse

Pulse 1 is the only channel that cannot be triggered on the start or end of a previous pulse.

User 1 Trigger Mode Register (VME: 0080h -> 0081h)

Purpose: Allows the operator to select the trigger mode for each of the eight channels while the V202 module is in User 1, or while the V202 module is in non-PPM mode.

This is a 16-bit read-write register. Each channel has its trigger mode determined by two bits within the User 1 Trigger Mode register. Bits D0 and D1 control channel 1. Bits D2 and D3 control channel 2, and so on.

The following bit pairs and their codes determine which trigger will be used for each channel:

D1	D0		Channel 1
D3	D2		Channel 2
D5	D4		Channel 3
D7	D6		Channel 4
D9	D8		Channel 5
D11	D10		Channel 6
D13	D12		Channel 7
D15	D16		Channel 1
0	0	=	Event Link
0	1	=	External
1	0	=	Start of previous channel pulse
1	1	=	End of previous channel pulse

User 2 Trigger Mode Register (Address 0082h -> 0083h)

Purpose: Allows the operator to select the trigger mode for each of the eight channels while the V202 module is in User 2.

This is a 16-bit read-write register. Each channel has its trigger mode determined by two bits within the User 2 Trigger Mode register. Bits D0 and D1 control channel 1. Bits D2 and D3 control channel 2, and so on.

The following bit pairs and their codes determine which trigger will be used for each channel:

D1	D0		Channel 1
D3	D2		Channel 2
D5	D4		Channel 3
D7	D6		Channel 4
D9	D8		Channel 5
D11	D10		Channel 6
D13	D12		Channel 7
D15	D16		Channel 1
0	0	=	Event Link
0	1	=	External
1	0	=	Start of previous channel pulse
1	1	=	End of previous channel pulse

User 3 -> User 8 Trigger Mode Registers (Address 0084h -> 008Fh)

Purpose: Allows the operator to select the trigger mode for each of the eight channels within User 3 through User 8.

The User 3 through User 8 Trigger Mode registers operate the same as the User 2 Trigger Mode register.

Output Mode Registers (Address 00A0h -> 00AFh)

A pulse output can be configured in one of four ways:

1) Output off low
2) Output active high
3) Output off high
4) Output active low

User 1 Output Mode Register (VME: 00A0h -> 00A1h)

Purpose: Allows the operator to select the output mode for each of the eight channels while the V202 module is in User 1, or while the V202 module is in non-PPM mode.

This is a 16-bit read-write register. Each channel has its output mode determined by two bits within the User 1 Output Mode register. Bits D0 and D1 control channel 1. Bits D2 and D3 control channel 2, and so on.

The following bit pairs and their codes determine which output mode will be used for each channel:

D1	D0		Channel 1
D3	D2		Channel 2
D5	D4		Channel 3
D7	D6		Channel 4
D9	D8		Channel 5
D11	D10		Channel 6
D13	D12		Channel 7
D15	D16		Channel 1
0	0	=	Output off low
0	1	=	Output active high
1	0	=	Output off high
1	1	=	Output active low

User 2 Output Mode Register (Address 00A2h -> 00A3h)

Purpose: Allows the operator to select the output mode for each of the eight channels while the V202 module is in User 2.

This is a 16-bit read-write register. Each channel has its output mode determined by two bits within the User 2 Output Mode register. Bits D0 and D1 control channel 1. Bits D2 and D3 control channel 2, and so on.

The following bit pairs and their codes determine which output mode will be used for each channel:

D1	D0		Channel 1
D3	D2		Channel 2
D5	D4		Channel 3
D7	D6		Channel 4
D9	D8		Channel 5
D11	D10		Channel 6
D13	D12		Channel 7
D15	D16		Channel 1
0	0	=	Output off low
0	1	=	Output active high
1	0	=	Output off high
1	1	=	Output active low

User 3 -> User 8 Output Mode Registers (Address 00A4h -> 00AFh)

Purpose: Allows the operator to select the output mode for each of the eight channels within User 3 through User 8.

The User 3 through User 8 Output Mode registers operate the same as the User 2 Output Mode register.

Gate Mode Registers (Address 00C1h -> 00CFh)

Normally, a channel operates in the ungated mode. This means that a pulse output is initiated by its specified trigger, and has a specified delay and width.

When a channel is set to the gated mode, its output is actually the result of gating the previous channel's output and its own programmed output. Only channel 1 cannot operate in gated mode.

As an example, assume that channel 2 is configured in gated mode. When pulse output 1 goes active, pulse output 2 also goes active. Pulse output 2 remains active until the channel 2 programmed trigger occurs, and the programmed delay expires. At that point, when pulse output 2 would normally go active, the pulse is reset. Channel 1 operates as it normally would.

If pulse outputs 2 through 7 were all set to gated mode, all 7 outputs would go active when pulse output 1 went active. The other 7 outputs would only end when their individual triggers occurred, and their delay counters expired.

It should be noted that a gated channel has its width counter forced to a value of 1, no matter what the programmed value is. This allows the width counters of a gated channel to expire and be reloaded as quickly as possible, allowing the channel to be ready for the next gated pulse.

User 1 Gate Mode Register (Address 00C1h)

Purpose: Allows the operator to select the gate mode for each of the eight channels while the V202 module is in User 1, or while the V202 module is in non-PPM mode.

This is an 8-bit read-write register. The high byte at VME address 00C0h doesn't actually exist. If an attempt is made to read these bit locations, the value returned will be indeterminate.

D0 controls pulse output 1. D1 controls pulse output 2, and so on. If a bit is set, the corresponding output is set to the gated mode. If a bit is "0", the corresponding output is in the ungated mode.

D0 of this register can physically be set, but it will be ignored. Pulse 1 cannot be operated in gate mode.

User 2 Gate Mode Register (Address 00C3h)

Purpose: Allows the operator to select the gate mode for each of the eight channels while the V202 module is in User 2.

This is an 8-bit read-write register. The high byte at VME address 00C2h doesn't actually exist. If an attempt is made to read these bit locations, the value returned will be indeterminate.

D0 controls pulse output 1. D1 controls pulse output 2, and so on. If a bit is set, the corresponding output is set to the gated mode. If a bit is "0", the corresponding output is in the ungated mode.

D0 of this register can physically be set, but it will be ignored. Pulse 1 cannot be operated in gate mode.

User 3 -> User 8 Gate Mode Register (VME: 00C5h -> 00CFh)

Purpose: Allows the operator to select the gate mode for each of the eight channels within User 3 through User 8.

The User 3 through User 8 Gate Mode registers operate the same as the User 2 Gate Mode register.

Delay And Width EPLD Memory (Address 0201h -> 05FFh)

Purpose: Allows the operator to load the delay and width values of each of the eight channels, within each of the eight users.

Each pulse output is derived from a 32-delay counter and a 32-bit width counter. Upon system initialization, a reset, arming, or expiration of an earlier pulse, the counters are loaded with values stored in RAM, which resides within the EPLD. When a trigger occurs, the delay counter counts down to zero, and the pulse output goes active. The width counter then counts down to zero, at which time the pulse ends. Upon completion of the pulse, the counters are reloaded with the original values. Reloading takes about 900 nanoseconds. The counters are then ready for another trigger.

Due to inherent device restrictions, the counter values are stored in the EPLD RAM in bytes widths. Each channel uses four bytes for delay, and four bytes for width. Since there may be up to 8 active users, sixty-four bytes of storage are needed for each channel. Eight channels then require a total of 512 bytes of memory storage.

The sixty-four bytes of delay and width values needed for each channel are stored in consecutive bytes. The eight bytes of User 1 delay and width values reserved for channel 1are followed by the eight bytes of User 2 delay and width values, and so on. That block of data is followed by channel 2's block of data, followed by channel 3's block of data, and so on.

A user's 32-bit delay and 32-bit width values for each channel are always stored MSB first. The first byte of the delay value contains bits 31 -> 24. The second byte contains bits 23 -> 16. The third byte holds bits 15 -> 8, and the last byte holds bits 7 -> 0. The width value is constructed identically to the delay value.

The smallest value a delay counter may be given is 00000000h. This means that when a trigger occurs, the pulse output will immediately go active. The largest value a delay counter may be given is FFFFFFFFh. This will provide a delay of 4,294,967,295 clocks.

The lowest value a width counter may be given is 00000001h. The pulse output must have some finite value, and 1 is the smallest allowable. The largest value a delay counter may be given is not actually FFFFFFFFh, but 00000000h. This is because the width counter will roll over. 00000000h will provide a width of 4,294,967,296 clocks.

See Appendix A for the address locations of each channel's delay and width values.

Event Link Look-Up Table External Memory (Address 1001h –> 1FFFh

Purpose: Allows the operator to configure a Look-up table that maps Event Link triggers to each of the eight channels, within each of the eight users.

The capability to trigger channels with the Event Link lies in the look-up table, implemented in external dual-port RAM.

An Event Link word contains 8 bits. Using each Event Link word as RAM address bits A7 -> A0, the 256-bytes of RAM are mapped so that specific Event Link words will result in data bits that can provide a triggering mechanism for each of the eight channels. The look-up table must be programmed in its entirety.

A value of "1" in RAM data bit D0 will trigger channel 1. A value of "1" in RAM data bit D1 will trigger channel 2, and so on. Ram data bits with a value of zero will not trigger a channel.

Using this method, it is possible for an Event Link word to trigger one output at a time, or up to all 8 outputs simultaneously. Of course, if the look-up table contains all zeroes at a particular location, no trigger will occur for that Event Link word.

The V202 module has provisions for up to 8 users. This means that there must be enough room in the RAM to provide eight separate 256-byte look-up tables. To address the separate look-up tables, the three user encoding bits are used as address lines A10 -> A8, providing access to a total of 2K of RAM.

The user encoding bits are coded as follows:

000 = User 1
001 = User 2
010 = User 3
011 = User 4
100 = User 5
101 = User 6
110 = User 7
111 = User 8

Since a dual-port RAM is used for the look-up table, the VME controller can access it at any time, without interrupting the on-board triggering process.

Because the RAM is only one byte wide, only the low bytes at the odd address locations exist. If an attempt is made to read the high bytes at even address locations, the values returned will be indeterminate.

See Appendix A for the address locations of each user's look-up table.

APPENDIX C

V202 Logic Descriptions

The V202 Logic Descriptions are referenced to sheet 1 and sheet 2 of the schematic identified by the drawing number 94028892.

Table Of Contents

Grounding Selections

Sheet 2 of drawing number 94028890

There are two main ground planes on the V202 module: digital ground and earth ground. These planes are on the same layer of the board, but they are split.

There are provisions onboard the V202 module to jumper the two main ground planes together, if so desired. This is done by shorting jumper headers JP11, JP12, and JP13.

In addition to the two main ground planes, each of the four front panel trigger input connectors, (J9 -> J12), as well as the front panel clock input connector, (J13) are positioned on their own mini-ground planes. Each of these five mini-ground planes is coupled to the earth ground through a .1-microfarad capacitor.

If desired, the coupling capacitor of each mini-ground can be bypassed. This connects the mini-ground directly to the earth ground. Shorting jumper header JP4 will connect the mini-ground of connector J9 directly to earth ground. Shorting jumper header JP5 will connect the mini-ground of connector J10 directly to earth ground. Shorting jumper header JP6 will connect the mini-ground of connector J11 directly to earth ground. Shorting jumper header JP7 will connect the mini-ground of connector J12 directly to earth ground. Shorting jumper header JP8 will connect the mini-ground of connector J13 directly to earth ground.

Event Link Input Buffering

Sheet 1 of drawing number 94028890

The Event Link is normally brought into the V202 module via J17, a front panel twinax connector. If the VME crate that holds the V202 is wired to accommodate it, the Event Link may also be acquired from backplane connect pins P2A-12 and P2A-13.

The front panel Event Link is transformer coupled with U3. The backplane Event Link is transformer coupled with U4. These are identical RF transformers, with a ratio of 1 and a frequency range of 400KHz to 800Mhz.

The output of transformer U3 is converted to TTL by U11, a low voltage PECL to TTL converter. The output of transformer U4 is converted to TTL by U12, another low voltage PECL to TTL converter.

The two outputs are made available at the 3-position jumper header JP2. Only one of the outputs can be jumped to the PLL circuit. If a jumper is placed on pins 1 and 2 of JP2, the front panel Event Link is selected. If a jumper is placed on pins 2 and 3 of JP2, the backplane Event Link is selected. If no jumper is in place, neither Event Link is connected

PLL Circuit

Sheet 1 of drawing number 94028890

The PLL circuit is a patented in-house design. It accepts the bi-phase mark encoded Event Link, and produces serial NRZ-L Event Link data, (Decoded_Data), along with a synchronized 10MHz clock, (Decoded_Clock). It also generates a synchronized 20MHz clock. The 10MHz clock is phased so that each positive going edge of the clock coincides with the middle of an Event Link data bit cell.

The center of the PLL circuit is U5, a programmable Altera device. The device may be programmed using Altera's Byte Blaster, connecting it to J15. The jumper must be removed from jumper header JP1 prior to connecting the Byte Blaster. Replace the jumper once U5 is programmed.

There are several support devices used in the PLL circuit.

VR1 is a 3.3V voltage regulator used to supply power throughout the PLL circuit, but nowhere else on the V202 module.

Y2 is an 11MHz reference oscillator used by U5.

U7 is an operational amplifier that controls the inhibit function of U8, an external VCO.

U8 is a VCO that provides U5 with a controlled 40MHz input.

U9 is voltage monitor. It makes sure that the PLL will operate only under the correct voltage conditions.

JP3 is a jumper header that must be shorted for proper operation.

External Triggers and External Clock Buffering

Sheet 2 of drawing number 94028890

There are four external trigger inputs available at the front panel. There is also one external clock input. The four external triggers are brought in on LEMO connectors J9, J10, J11, and J12. The external clock is brought in on LEMO connector J13.

Each one of the five inputs is referenced to its own mini-ground, which is coupled to earth ground with a .1uf capacitor. Each capacitor can be shorted with a jumper, essentially connecting the mini-ground directly to earth ground. JP4 shorts J9's mini-ground, JP5 shorts J10's mini-ground, JP6 shorts J11's mini-ground, JP7 shorts J12's mini-ground, and JP8 shorts J13's mini-ground.

Each of the external inputs is optically isolated from the V202 module using high-speed optocouplers. U19 isolates the J9 input, U20 isolates the J10 input, U21 isolates the J11 input, U22 isolates the J12 input, and U23 isolates the J13 input.

Each input is converted to an active low TTL level signal. The signals are then buffered by U40, a hex inverter, and presented to U37 for processing.

Pulse Output Buffering

Sheet 2 of drawing number 94028890

There are eight pulse outputs available at the front panel. They are brought out on LEMO connectors J1 through J8.

The pulses themselves are generated inside U37, an Altera programmable device that is the heart of the V202 module. The pulses are labeled P1 through P8. P1, P2, and P3 are buffered by U1. P4, P5 and P6 are buffered by U15. P7 and P8 are buffered by U17.

Each device has three drivers and three receivers. The receivers are not used. The outputs all have short circuit protection. They may be wire-ORed, but the outputs must not be programmed for inverted operation if doing this. All outputs are TTL compatible.

AGS Clock Buffering

Sheet 2 of drawing number 94028890

The AGS clocks are short, active low strobes. They are generated inside U37, an Altera programmable device that is the heart of the V202 module.

They are buffered by U32, a quad differential line driver. The AGS clock strobes are driven differentially and presented to the backplane connector pins P2A-16 through P2A-23. These clocks are used by the AGS to TTL Converter.

VME Buffering

The V202 module is a VME bus slave. It accommodates both read and write data transfers. VME data is read and written directly to both U37, an Altera programmable device that is the heart of the V202 module, and U35, a dual-port RAM used to hold the Event Link look-up table.

To support the VME data transfers, a number of buffers are used to allow the V202 module to interface with the VME control lines, address lines, and data lines.

Twenty-four address lines, A23 -> A1, are buffered by U24, U25, and U26. These devices are octal D-type registers. They are enabled at all times, because the address lines are only driven by the VME controller.

The address modifier lines, AM5 -> AM0, as well as *LWORD and *IACK are buffered by U27, another octal D-type register.

U24, U25, U26, and U27 are clocked by a signal named DS. DS is derived by NANDing the buffered *DS0 and *DS1 signals inside U33. U33 contains four 2-input NAND gates.

Sixteen data lines, D15 -> D0, are buffered by U29 and U30. These devices are octal bus transceivers. The devices are enabled and steered (data flow in or out of module) by signals generated in U37.

*DTACK and *IRQ1 through *IRQ7 are driven onto the VME backplane by U31. This device is an open collector transceiver capable of driving the outputs with 48mA. The device is always steered to drive the lines out of the module.

*DS0, *DS1, *IACKIN, *WRITE, and *SYSRST are VME control line inputs that are buffered by U28. This device is an octal line driver.

*IACKOUT, a signal driven onto the VME bus, is also buffered by U28.

*AS is buffered by U40, which also inverts the signal.

Base Address Decoding

The base address of each V202 module is set with SIP switch SW1.

The upper VME address bits, A23 -> A16, which have been buffered by U24, are presented to U36 for decoding. U36 is an 8-bit comparator, SN74LS682DW. The address bits are compared to the outputs of SIP switch SW1. When the two sets of bits match, the signal /ADDR_COMP goes low. This signal indicates that the current VME data transfer is meant for the V202 module.

Jumper header JP9 provides the means to populate the V202 module with a different comparator, in case the SN74LS682DW becomes unavailable. U36 can be replaced with a SN74ALS520DW, but JP9 must be shorted when this device is used. Normally, when a SN74LS682DW is installed JP9 must be open.

Setting The V202 Module's Serial Number And Revision Letter

The V202 module's serial number and revision letter can be obtained over the VME bus by reading the onboard VME ID message. This message is generated by U37, an Altera programmable device that is the heart of the V202 module.

To set the serial number and revision number of each module without having to reprogram each device, two onboard Shorting Sockets must be configured prior to installation. The information from each shorting socket is presented to U37, which translates the data into a serial number and revision letter.

SS1 is an 8-position socket, which represents the board's serial number. When all the shorting positions are left open, the board's serial number will be 1. When the LSB of the shorting socket is shorted, the board's serial number will be 2, and so on. The 8-position socket allows for serial numbers 1 through 256.

SS2 is a 3-position socket, which represents the board's revision letter. When all the shorting positions are left open, the board's revision letter will be A. When the LSB of the shorting socket is shorted, the board's revision letter will be B, and so on. The 3-position socket allows for revision letters A through H.

Pulse Configuration And Control

Almost all of the operations of the V202 module are controlled by U37, the heart of the V202 module. U37 is an Altera device, EP1K100QC208-1. The only pulse control function that resides outside this device is the Event Link look-up table, which resides in U35.

U37 requires two different voltages. The internal logic functions operate on 2.5V. The I/O of U37 utilizes 3.3V, which makes the I/O TTL compatible. VR2 supplies the 3.3V. VR3 supplies the 2.5V.

U37 utilizes a free-running system clock that is used for a host of internal logic functions. Y1 is a 20MHz oscillator that provides this clock. It is not associated with the 20MHz clock derived in the PLL circuit.

U34 is a configuration device that downloads the program into U37 each time power is first applied to the board. U34 is programmed with an Altera Byte Blaster, which is connected to J14 during programming. U37 can also be programmed this way, but it loses its program when power is removed. U34 does not.

U34 gets configured with a .pof version of the program. U37 gets configured with an .sof version of the program.

Some, but not all of the module functions controlled by U37 are listed below:

1) Clock selection and distribution
2) VME read/write interface
3) Interrupt generation
4) VME interrupt interface
5) Event Link decoding
6) Trigger control
7) Gate mode control
8) Output mode control
9) Pulse reset control
10) User switching and control
11) Pulse delay and width control

The Event Link look-up table resides in U35, a 2K dual-port RAM device. U35 has two sets of data lines and two sets of address lines. Buffered VME data lines and address lines control the configuration of the look-up table, which is essentially a trigger map. Decoded Event Link words and user coding bits are used as the other set of address lines to the RAM, whose look-up table data is presented to U37 for Event Link trigger processing.

LED Control

There are twelve LEDs visible on the front panel of the V202 module.

Power

The green POWER indicator is tied directly to the +5V power acquired from the VME backplane.

VME

The green VME indicator is driven by U18, a dual precision timer that pulse stretches its input. The timer input is derived from *DTACK, a short negative going strobe that occurs each time a VME data transfer occurs between the V202 module and the VME controller.

Event Link

The green EVENT LINK indicator is driven by U18, a dual precision timer that pulse stretches its input. The timer input is pulsed low each time a valid Event Link word is decoded. Under normal working conditions with an active Event Link, this LED will be constantly illuminated. It will never be on when the red NO LOCK indicator is on.

No Lock

The red NO LOCK indicator turns on when the V202 module's PLL is not synchronized to the Event Link. It is driven by U28. Under normal working conditions, when the PLL is locked to the Event Link, this indicator will not be illuminated.

Pulse Outputs

A timer drives each of the eight small green pulse activity indicators. Each timer's input is a negative strobe that has the same duration as the corresponding pulse output. The timers pulse stretch their inputs, so even a short pulse output will cause its corresponding LED to be illuminated long enough to be seen.

U2 drives the LEDS for pulse output 1 and pulse output 2. U13 drives the LEDS for pulse output 3 and pulse output 4. U14 drives the LEDS for pulse output 5 and pulse output 6. U16 drives the LEDS for pulse output 7 and pulse output 8.